

Switched-Capacitor Resonant DC–DC Converter with Differential Power Processing for Stacked Servers in Data Center Applications

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Abstract—This paper presents an alternative approach for efficient DC power distribution and voltage regulation in data centers. A switched-capacitor (SC) resonant DC–DC converter with differential power processing (DPP) is proposed, enabling servers to be electrically connected in series. This configuration inherently steps down the voltage from a higher-voltage DC bus, where voltage regulation for each server is achieved using SC half-bridge cells that process only the differential (mismatch) power between servers, while the bulk power is transferred without active processing. It results in notably improved system efficiency compared to conventional architectures. Additional features of the proposed converter include its simplicity due to open-loop operation, soft-switching capability, and tolerance to hot-swapping of servers. Here, the concept is demonstrated and validated through circuit simulations considering a test system comprising a series-stacked server rack with four 12 V servers powered from a 48 V DC bus, delivering up to 600 W.

Keywords—Data center, Differential power processing, Hot-swapping, Resonant DC–DC converter, Switched-capacitor.

I. INTRODUCTION

Over the past decades, technological advancements in semiconductors, circuits, and system architectures have driven substantial progress in power electronics [1], with static power converter efficiencies recently approaching 99% in various applications. One of the main concepts contributing to this improvement is the partial power processing (PPP) [2], [3], which can be categorized into two main approaches: parallel current regulators (PCRs) and also series voltage regulators (SVRs). The former gives rise to differential power processing (DPP) architectures [4], while the latter gives rise to series-connected partial power converters (S-PPCs) [5], [6].

DPP systems have emerged as promising solutions for efficient power delivery across a wide range of applications [7]. They have been applied to photovoltaic (PV) systems to mitigate current mismatch and enable maximum power point tracking (MPPT) for series-connected PV modules [8], [9]; to battery/supercapacitor strings as active equalization circuits [10]; and more recently, to minimize conversion effort in emerging DC applications such as data center servers [11], unmanned aerial vehicle (UAV) charging stations [12], and microprocessor systems [13]. In DPP architectures, converter cells process only a small fraction of the total power during normal operation, which leads to improved system efficiency and reduced converter size [14]. In other words, these series-stacked architectures enable the DPP cells to process only the mismatch current instead of the full current of the power supply or load. Various implementations of the series-stacked DPP architecture concept are discussed in [15].

This paper proposes a fully DC-coupled, non-isolated Dickson-based switched-capacitor (SC) DPP converter with *LRC* resonance, intended for data center applications. The proposed solution is developed as part of the *Data Centre Demonstrator* project, supported by the *Shift2DC* initiative under the *Horizon Europe* program. As illustrated in Fig. 1, the demonstrator schematic includes a black-box DC–DC converter representing the power conversion module under development by TalTech – Tallinn University of Technology for server power delivery. In summary, the proposed module consists of two main stages: (1) a high step-down, isolated full-power converter (FPC) and (2) a non-isolated SC-based DPP converter that performs PPP.

The Dickson-based SC DPP converter is proposed for use in the second stage, with the primary goals and objectives of its implementation being:

- Achieve high efficiency by reducing power losses;
- Ensure high power density for compactness;
- Enable hot-swapping capability with uninterrupted power delivery and voltage regulation;
- Provide device failure protection by treating failure conditions as hot-swap events;
- Implement soft-start to limit inrush current spikes during swapping in;
- Maintain safety isolation for floating servers.

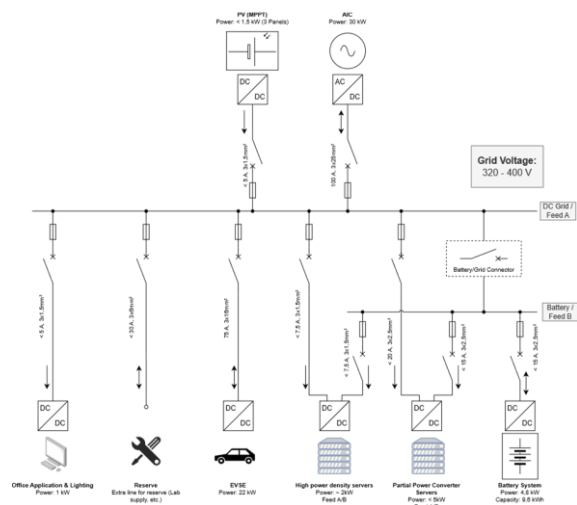


Fig. 1. Diagram of the *Data Centre Demonstrator* project, supported by the *Shift2DC* consortium under the *Horizon Europe* program.

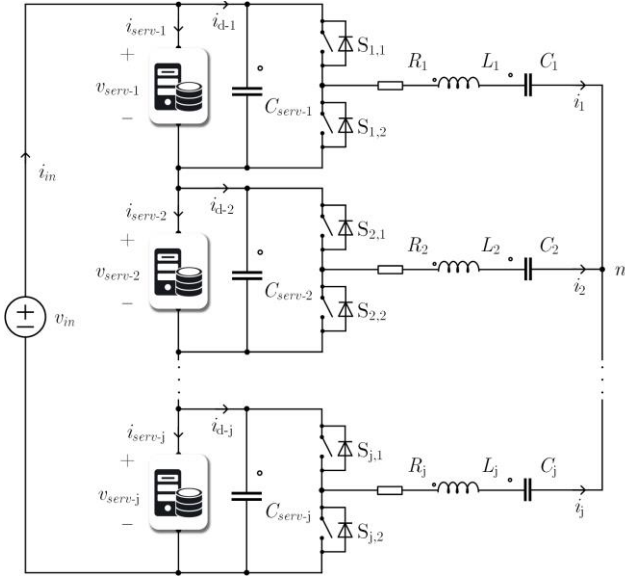


Fig. 2. Proposed Dickson-SC DPP topology for data center applications.

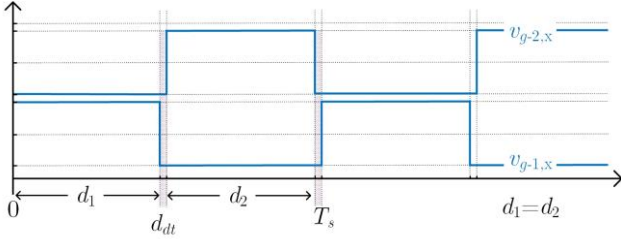


Fig. 3. Control signals and time slots of the SC cells.

II. DICKSON-SC DPP FOR DATA CENTERS

This section outlines the principles of DPP and presents the proposed Dickson-SC DPP converter designed for data centers. It discusses the power converter topology, operating principles, and main advantages in addressing the specific power demands of data center applications.

A. DPP for data center applications

The first stage of the double-stage module shown in Fig. 1 is a dual-active bridge (DAB) converter [16]. This converter is responsible for stepping down the high input voltage (320–400 V), supplied by feeds *A* (DC grid) and *B* (battery system), to a regulated 48 V DC bus. Complementing this stage, the second DC–DC converter is the proposed fully DC-coupled, non-isolated Dickson-SC DPP converter with *LRC* resonance operation, which is illustrated in Fig. 2. In that module, it operates connected to the 48 V DC bus and supplies a series-stacked load composed of $j = 4$ server domains connected in series (*i.e.*, each domain operates at 12 V). To the best of the authors' knowledge, this is the first application of a Dickson-SC DPP converter in data centers.

Compared to a conventional FPC that must process the full power in the second stage [7], the main advantage of DPP architectures is that the i -th SC cell in the series stack ideally processes only the amount of active power resulting from the current mismatch between the DC bus and the i -th server [15]. Consequently, the total active power processed (P_{proc}) by the Dickson-SC DPP converter remains very low when all servers are operational and consuming similar amounts of power. In this case, the majority of the active power is delivered directly to the loads, while only a small power difference is processed

through the DPP cells [11]. The power processed increases only in response to variations in the individual active power consumption of each server in the series stack.

Considering the schematic diagram of the Dickson-SC DPP converter shown in Fig. 2 (and assuming that it is ideal), where i refers to any server and j represents the total number of servers in steady-state operation, by applying Kirchhoff's Voltage Law (KVL) around the series stack and Kirchhoff's Current Law (KCL) at each intermediate node result in [18]

$$v_{in} = \sum_{i=1}^j v_{serv-i} \quad (1)$$

$$i_{in} = i_{serv-i} + i_{d-i}. \quad (2)$$

Assuming that all the series-stacked server voltages are regulated to their nominal values ($V_{serv,nom}$) over a general period (T_s), averaging (1) and (2) over T_s results in [18]

$$V_{in} = \sum_{i=1}^j V_{serv-i} = j \times V_{serv,nom}, \quad (3)$$

$$I_{in} = \frac{1}{j} \times \sum_{i=1}^j I_{serv-i}. \quad (4)$$

Therefore, if the server voltages are regulated to their nominal values, the average power processed by the DPP cells (*i.e.*, the total power processed by the system) is given by

$$P_{proc} = V_{serv,nom} \times \sum_{i=1}^j |I_{in} - I_{serv-i}|. \quad (5)$$

Complementarily, the total power delivered to the servers by the Dickson-SC DPP converter is given by

$$P_{deliv} = V_{serv,nom} \times \sum_{i=1}^j I_{serv-i}. \quad (6)$$

Therefore, unlike ladder-based DPP converters [14], the active power processed in a Dickson-based DPP converter is not cumulative [15], [17]. Ideally, each cell transfers only the amount of active power required to compensate for current imbalances, supplying or absorbing active power as needed. By processing only the power resulting from the mismatches, power losses in the second stage can be significantly reduced, thereby improving the overall system efficiency. Moreover, because less active power is processed, the converter rating requirements, cost, weight, and size can also be reduced compared to state-of-the-art designs.

Even though hot-swapping or server failure (where some servers are completely isolated from the series stack while others remain operational) occurs during a relatively small portion of the operating time, such events result in abnormal power imbalances for the remaining servers (increasing the total power processed) and must be accounted for in data centers. Since the Dickson-SC DPP converter operates as a transformerless voltage equalizer DC–DC converter using a fixed switching frequency and duty cycles, it can continue to operate reliably even during such events. Derivations of the previous equations and analyses in this section, considering hot-swap scenarios, can be found in [18].

B. Operating principles of the proposed converter

As shown in Fig. 2, the proposed converter consists of multiple bidirectional half-bridge cells, each comprising an *LRC* coupling network and a pair of transistors ($S_{i,1}$ – $S_{i,2}$). The

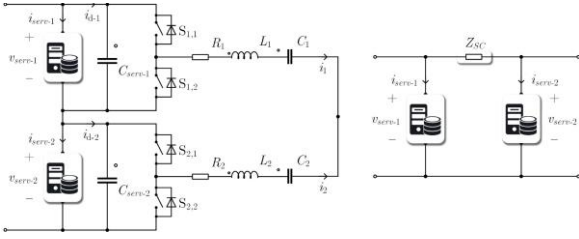


Fig. 4. Dickson-SC dc-dc topology with two SC cells.

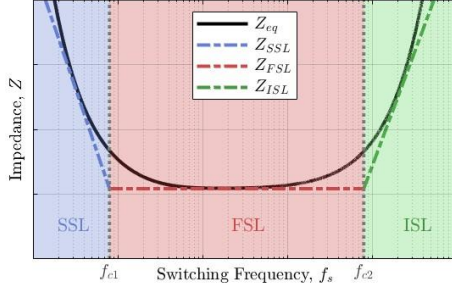


Fig. 5. Equivalent impedance of the Dickson-SC with two cells.

main advantage of this converter is that it eliminates the need for bulky magnetic components, as the voltage domains are coupled through passive elements [15], where the inductors used are relatively small and primarily serve to generate resonant waveforms and enable soft-switching operation. In addition, the converter features a reduced switch count and/or fewer differential power conversion stages compared to other existing DPP solutions [10], [14], [18], reducing the total cost and size. This occurs because the proposed converter directly transfers power between arbitrary DPP cells using simple “DC–AC–DC” power stages. From cell to cell, the converter operates effectively as a one-to-one converter.

The SC voltage-balancing operation is achieved through complementary gate signals applied to each transistor pair, with an appropriate dead time (d_{dt}) to prevent shoot-through. Consequently, the Dickson-SC DPP converter operates with two equal duty cycles, denoted as d_1 and d_2 , as illustrated in Fig. 3. With proper design, therefore, all switches can achieve zero-current switching (ZCS) at turn-on due to the limited current rise (di/dt), and zero-voltage switching (ZVS) at turn-off, both across the entire operating range. This minimizes switching losses and further improves efficiency.

Considering four server domains connected in series, the voltage across the two inner resonant capacitors is ideally $V_{Ci} = 0.5 \times V_{serv,nom}$, while the voltage across the outer capacitors is $V_{Ci} = 1.5 \times V_{serv,nom}$. Additionally, the upper capacitors (C_1 and C_2) have opposite voltage polarity compared to the lower capacitors (C_3 and C_4). The voltage across the output filter capacitors (C_{serv-i}), as well as the blocking voltage of the active switches, is equal to the server voltage.

III. CONVERTER DESIGN AND OPTIMIZATION

The concepts of slow switching limit (SSL), fast switching limit (FSL), and inductive switching limit (ISL), as discussed in [17], are applied here to optimize the performance of the proposed Dickson-SC DPP DC–DC converter by minimizing the value of the equivalent impedance (Z_{eq}) that represents the total effective impedance of the converter components.

A. Approach for equivalent impedance minimization

To ensure proper operation and simultaneously optimize the performance of the proposed Dickson-SC DPP topology,

considering here the circuit with two cells and its behavioral model illustrated in Fig. 4 [17], the quality factor (Q) should be less than 1 (preferably below 0.5), where

$$Q = \sqrt{(L_i/C_i)/R_i}. \quad (7)$$

In addition, the design of the Dickson-SC converter should also adhere to the following guidelines [17]:

1. Minimize all parasitic resistances to reduce the FSL impedance (Z_{FSL}), which is equal to $8R_i$.
2. Set the switching frequency (f_s) as close as possible to the first crossover frequency (f_{c1}) given by

$$f_{c1} = 1/(4R_iC_i), \quad (8)$$

to minimize the equivalent impedance and to reduce both switching and gate-drive losses.

3. Minimize stray inductances to ensure that the second crossover frequency (f_{c2}), defined as

$$f_{c2} = R_i/4L_i, \quad (9)$$

remains higher than f_s , thereby avoiding performance degradation due to inductive effects.

Fig. 5 illustrates the equivalent impedance of the circuit with two cells illustrated in Fig. 4, along with its simplified model, as a function of the switching frequency, where

$$Z_{SSL} = 2/(f_s C_i), \quad (10)$$

$$Z_{ISL} = 32f_s L_i, \quad (11)$$

$$Z_{eq} = 2Z_{SC}, \quad (12)$$

while the full expression of Z_{SC} can be found in [19], which is the combination of the RLC parameters at the same time.

As can be seen in Fig. 5, Z_{eq} rises along with the decrease in the switching frequency below f_{c1} , whereas the opposite takes place above f_{c2} . This behavior provides insights into the performance under different conditions and is essential for optimizing efficiency by selecting an appropriate switching frequency. The minimum equivalent impedance is shown to occur between the two crossover frequencies.

IV. SIMULATION RESULTS AND DISCUSSIONS

To validate the proposed converter, simulations have been conducted using the PSIM[®] software. Table I presents the electrical specifications relevant to the data center application. Although $j = 4$ in this instance, the Dickson-SC DPP converter is scalable to a greater number of servers connected in series. In contrast, Table II outlines the set of specifications used in the simulations, where the servers were modeled as resistive loads. These parameters were selected to reflect realistic operating conditions and served as the basis for evaluating the converter's performance. To support hot-swapping operations, the SC cells have been rated for the full server power [18].

Based on this, Fig. 6(a) presents the simulated voltage and current waveforms for the servers and RLC components of the Dickson-SC DPP converter under conditions of low current mismatch. In contrast, Fig. 6(b) shows the simulation results for the same components during a hot-swap event involving

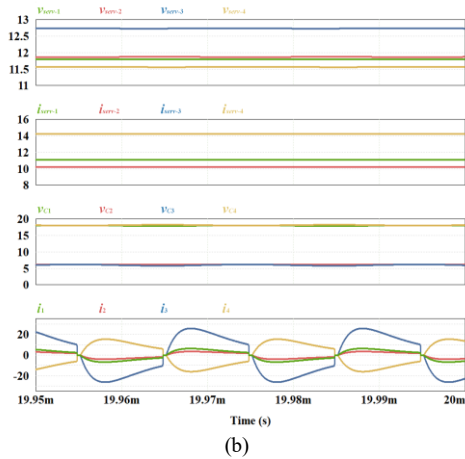
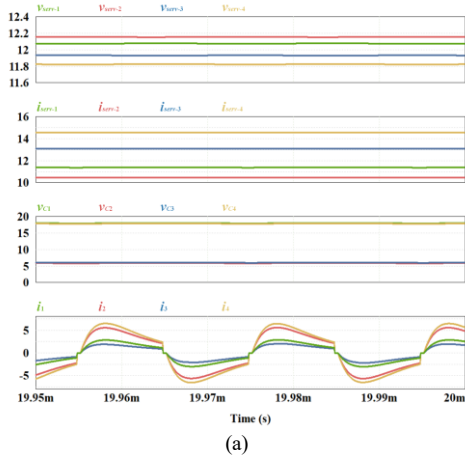


Fig. 6. Simulation results: (a) under low current mismatch conditions; (b) during the hot-swap of server 3.

server 3, which leads to an increase in circulating currents due to higher active power processing. Under this latter condition, Fig. 7 highlights the ZCS turn-on operation capability of the switches in the proposed converter.

Fig. 8 presents the simulation results in which a hot-swap event occurs for server 3 at 13 ms. Despite this disturbance, the converter continues to operate correctly, with the output voltage of the corresponding cell rising and stabilizing below 13 V, an acceptable range for server operation. This behavior is attributed to the system operating in open-loop mode during the hot swap event, where the voltages adjust dynamically to meet power demands. After a brief interval, server 3 is fully integrated and the system returns to its previous operating point, characterized by low power processing. These results demonstrate the robustness of the converter under dynamic conditions typical of data center environments, although in practical applications, hot swapping can induce large current transients due to the high capacitance of servers [14].

Fig. 9(a) shows the 3D model of the converter designed in Altium®, while Fig. 9(b) shows a photograph of the physical prototype, which measures 20 cm × 16.5 cm and supports up to 600 W of system power. The complete list of part numbers used in that prototype is provided in Table III. Experimental results, along with additional analysis and discussion, will be presented in the final version of the paper.

V. CONCLUSION

This paper proposed a resonant SC converter with DPP as an efficient solution for DC power distribution and voltage

TABLE I. SPECIFICATIONS FOR THE DATA CENTER APPLICATION

Param.	Value	Unity
j	4	Un.
$V_{serv,nom}$	12	V
$R_{serv,nom}$	0.96	Ω
$P_{serv,nom}$	150	W
$P_{in,nom}$	600	W
V_{in}	48	V
d_1, d_2	0.48	–
d_{dt}	0.02	–
f_s	50	kHz

TABLE II. SPECIFICATIONS OF THE PROPOSED CONVERTER

Param.	Value	Unity
Q	0.42	–
L_i	23.5	nH
R_i	18.5	m Ω
C_i	390	μ F
f_{c1}	34.65	kHz
f_{c2}	196.81	kHz

TABLE III. SPECIFICATIONS FOR THE EXPERIMENTAL PROTOTYPE

Parameter	Part number
Switches	BSC009NE2LS5IATMA1
Heatsinks	FK 250 06 LF PAK
C_{serv-i} (aluminum)	4 mF, 4x EEH-ZU1E102UP
C_{serv-i} (ceramic)	40 μ F, 4x CL32A106KLULNNE
C_i (inner)	408 μ F, 6x KCM55WR71E686MH01K
C_i (outer)	600 μ F, 6x CKG57NX7R1V107MT*
L_i	23.5 nH, 1010VS23NMEC
DSP	LAUNCHXL-F28379D

regulation in data centers. By enabling series-stacked server configurations powered from a common DC bus, the proposed architecture facilitates bulk active power transfer without power processing and employs SC cells to regulate differential power among servers. This approach significantly improves overall efficiency compared to conventional approaches and architectures. The converter incorporates a simplified open-loop control scheme, full-range soft-switching capability, and also inherent robustness to hot-swap events. The concept has been validated through simulations of a system consisting of four 12 V servers connected in series and supplied by a 48 V DC bus, confirming the feasibility and effectiveness of the proposed solution for next-generation data centers.

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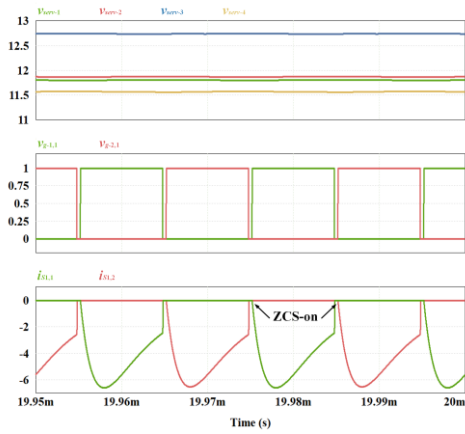


Fig. 7. Demonstration of the ZCS capability of the proposed converter.

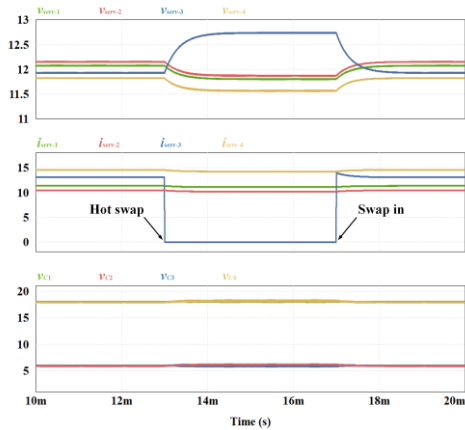
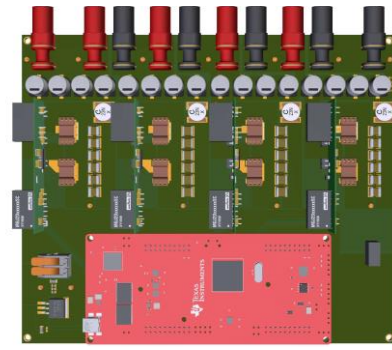


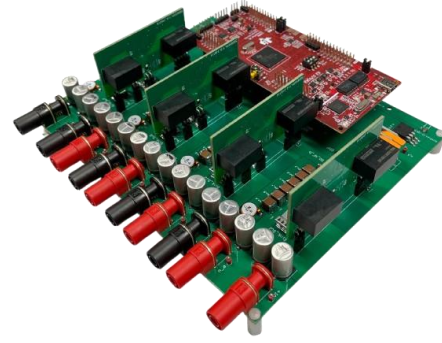
Fig. 8. Simulation results showing the output voltage of each server and the voltages across the RLC components during the hot-swap of server 3.

REFERENCES

- [1] N. G. F. dos Santos, J. R. R. Zientarski, and M. L. d. S. Martins, "A review of series-connected partial power converters for DC–DC applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7825–7838, Dec. 2022.
- [2] N. Yadav, A. Chub, N. Hassanpour, A. Blinov, D. Vinnikov, and I. Galkin, "A hybrid modulation approach for step-up/down partial power converter with improved MPPT efficiency around zero partiality," *IEEE Trans. Ind. Appl.*, vol. 61, no. 2, pp. 3259–3268, Apr. 2025.
- [3] N. G. F. dos Santos, A. Toebe, P. H. B. Löbler, L. Schuch, M. L. da S. Martins, and C. Rech, "A high-efficient single-switch switched-capacitor partial power converter for on-board chargers," *IEEE Trans. Power Electron.*, vol. 39, no. 11, pp. 15269–15280, Nov. 2024.
- [4] P. S. Shenoy and P. T. Krein, "Differential power processing for DC systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1795–1806, Apr. 2013.
- [5] N. G. F. dos Santos, J. R. R. Zientarski, and M. L. da S. Martins, "A ZCS/ZVS DC–DC partial power converter with reconfigurable H-bridge and variable turns ratio for an integrated on-board charger," *IEEE Trans. Power Electron.*, vol. 39, no. 10, pp. 13916–13933, Oct. 2024.
- [6] E. L. Carvalho, A. Chub, N. Hassanpour, A. Blinov, A. K. Rathore, and D. Vinnikov, "P3R: Partial power post-regulated grid-forming converter for prosumer DC buildings," *IEEE Trans. Ind. Electron.*, vol. 72, no. 2, pp. 1628–1637, Feb. 2025.
- [7] P. Wang and M. Chen, "Analysis and design of series voltage compensator for differential power processing," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 7890–7903, Dec. 2022.
- [8] M. Uno and T. Shinohara, "Module-integrated converter based on cascaded quasi-Z-source inverter with differential power processing capability for photovoltaic panels under partial shading," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11553–11565, Dec. 2019.



(a)



(b)

Fig. 9. Proposed DC–DC converter implementation: (a) 3D model designed in Altium®; (b) photograph of the experimental prototype.

- [9] J.-H. Lim, D.-I. Lee, Y.-J. Hyeon, and H.-S. Youn, "Differential power processing converter with active clamp structure and integrated planar transformer for power generation optimization of multiple photovoltaic submodules," *IEEE Access*, vol. 11, pp. 5668–5678, 2023.
- [10] Y. Ye and K. W. E. Cheng, "Modeling and analysis of series–parallel switched-capacitor voltage equalizer for battery/supercapacitor strings," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 4, pp. 977–983, Dec. 2015.
- [11] P. Wang, Y. Chen, J. Yuan, R. C. N. Pilawa-Podgurski, and M. Chen, "Differential power processing for ultra-efficient data storage," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4269–4286, Apr. 2021.
- [12] M. Liao *et al.*, "UAV fleet charging on telecom towers with differential capacitive wireless power transfer," *IEEE Trans. Power Electron.*, vol. 40, no. 4, pp. 6370–6384, Apr. 2025.
- [13] C. Schaefer and J. T. Stauth, "Efficient voltage regulation for microprocessor cores stacked in vertical voltage domains," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1795–1808, Feb. 2016.
- [14] A. Stillwell and R. C. N. Pilawa-Podgurski, "A resonant switched-capacitor converter with GaN transistors for high-efficiency power delivery to series-stacked processors," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 3139–3150, Sept. 2020.
- [15] P. Wang, R. C. N. Pilawa-Podgurski, P. T. Krein, and M. Chen, "Stochastic power loss analysis of differential power processing," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 81–99, Jan. 2022.
- [16] E. L. Carvalho, A. Sidorova, A. Blinov, A. Chub, and D. Vinnikov, "Design considerations of dual-active bridge DC grid-forming converter for DC buildings," *IEEE Trans. Ind. Electron.*, vol. 71, no. 9, pp. 10601–10611, Sept. 2024.
- [17] Y. Ye, K. W. E. Cheng, Y. C. Fong, X. Xue, and J. Lin, "Topology, modeling, and design of switched-capacitor-based cell balancing systems and their balancing exploration," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4444–4454, Jun. 2017.
- [18] E. Candan, D. Heeger, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Hot-swapping analysis and implementation of series-stacked server power delivery architectures," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 8071–8088, Oct. 2017.
- [19] M. Uno, H. Sato, and S. Oyama, "Switched capacitor-based modular differential power processing architecture for large-scale photovoltaic systems under partial shading," *IEEE Trans. Energy Convers.*, vol. 37, no. 3, pp. 1545–1556, Sep. 2022.