Performance Evaluation of Step-Up/Down Partial Power Converters Based on Current-Fed DC-DC Topologies

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***Abstract*—This paper presents several topologies of the series-connected partial power converters based on current-fed full-bridge and push-pull topologies. It provides a detailed comparison of the voltage and current stresses of the components and analyzes the controllability of the corresponding converters near zero partiality. The analysis is performed for the same operating conditions to define performance traits of the baseline current-fed topologies in the partial power conversion systems. The experimental study corroborates the theoretical results. An application-agnostic comparative assessment for these topologies is provided. Their performance in PV applications was demonstrated as a case study. All the results are obtained for converter operation in a residential dc microgrid with an operating voltage of 350 V and considering PV string voltage range of 350 $\pm$ 50 V, which results in the maximum partiality of 12.5%.**

***Index Terms*—Dc-dc converter, full-bridge converters, modulation, partial power converter, push-pull converters.**

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I. Introduction

DEMANDS imposed on modern electric energy generation and distribution networks have sped up the development of power electronic systems [1]. Due to the widespread adoption of domestic solar photovoltaic (PV) and wind power systems, the technology of residential battery energy storage systems has attained the most interest among the rest [2], [3]. Power converters interface these energy generation and storage units, making them especially important in dc microgrids [4]. These converters can be broadly categorized into voltage-fed, impedance-source, and current-fed (CF) converters [5], [6], [7]. Recently, current-fed converters have been introduced because of their inherent benefits, such as soft switching [8], [9], resonant switching [10], use of parasitic resonance [11], and active snubber [12].

Dual active bridge (DAB) is a dependable and frequently used technology that offers soft switching, good scalability, and high efficiency in a limited voltage and power range [13]. Recent research targeted applications with a wide output voltage range for universal electric vehicle charging due to the emergence of 800 V powertrain [14], [15].

Recent research has led to a new kind of galvanically isolated soft-switching CF topologies, which comprise secondary-side switches that are actively controlled synchronously with the primary-side four-quadrant switches [16], [17], [18]. Their best implementations in [19], [20] employ an improved quasi-resonant modulation with significantly reduced ringing and turn-off losses.

The biggest shortcoming of the full-bridge soft-switching CF topologies is the high number of switches on the CF side. In order to overcome such shortcomings, CF topologies with a reduced number of switches, such as the push-pull dc-dc converter [21], [22], [23], could be used. A push-pull dc-dc converter presented in [23] was designed for household applications. It features the number of CF-side switches reduced from eight to four. Even though the push-pull CF topologies suffer from increased voltage stress of switches, they can enhance the converter efficiency or reduce the cost in some applications.

Since full power converters have been around for a while, their efficiency has reached feasibility limits defined by the limitations of the passive and semiconductor component technologies. Though several studies aim to improve efficiency, full

power processing has little room for improvement. Recently, an innovative concept of partial power converters (PPCs) has emerged to maximize efficiency to the level that cannot be achieved with conventional full power converters [24], [25], [26], [27], [28], [29]. Unlike full power converters, a PPC uses a small portion of the system power for load regulation. This results in high conversion efficiency (η_{PPC}), high power density, and reduced power rating of components. These distinctive characteristics make PPC well-suitable for electric vehicles, PV systems, battery storage systems, and fuel cell applications [30].

Most case studies on PPCs carried out in recent years are based on configurations such as parallel current regulators, series voltage regulators, and series-connected partial power converters (S-PPC). S-PPCs could be broadly categorized into step-up, step-down, and step-up/down converters [27]. A current-fed full high-frequency link inverter-based PPC is presented in the [31], which comprises the two-quadrant switches at series port (SP), also known as low-voltage port. However, hard switching is presented, which decreases the system efficiency. In [26], another bidirectional step-up/down CF S-PPC is introduced, incorporating soft switching and offering reduced component stress. Another PV application-oriented PPC is reported in [32], where an issue with mode transitions using conventional phase shift modulation (PSM) was demonstrated along with a possible solution to tackle this challenge.

As per the above discussion, it can be summarized that CF full bridge based PPCs feature a high number of switches at the SP side and have some constraints in the mode transition with conventional PSM. The push-pull topologies can overcome such issues, which resulted in the derivation of a push-pull PPC in [33], where only basic principles are demonstrated. In this paper, the push-pull CF-based PPC from [33] is analyzed in detail by considering the aforementioned aspects. By benchmarking all possible modulation techniques applicable to the given push-pull PPC and comparing their performance with the corresponding baseline full-bridge PPC, this paper offers a push-pull PPC with improved characteristics compared to those in [33]. This paper considers PV applications to exemplify how the PPC modes (step-up and step-down) change due to the ambient temperature variations. Conclusions drawn from this case study could be extended to other applications.

The literature review yielded that CF topology-based PPCs perform best in step-up/down applications with minimum partiality. On the other hand, the performance of CF full-bridge and push-pull topologies was never studied in step-up/down PPC applications. The main contributions of the paper are as follows:

1) A novel push-pull-based PPC is introduced along with a novel quasi-resonant modulation, which offers higher converter efficiency as compared to push-pull-based PPC from [33] and full bridge-based PPCs from [26], [32].
2) A resonant-based modulation for push-pull PPC is demonstrated, which allows the PPC to function with complete zero voltage switching (ZVS) turn-on and zero current switching (ZCS) turn-off.
3) Application type is the only factor that influences PPC configuration choice. In this paper, the PV application uses a bi-directional configuration. This case study was created to show how well MPPT performed with push-pull PPC and FB-HFLI. However, the comparative evaluation that this article provides considers bidirectional configuration and is done in a generalized manner.
4) The proposed push-pull PPC is demonstrated for PV applications under varying PV cell temperatures to justify the usability of the proposed concept.
5) The performed comparative study employs theoretical and experimental validation of different modulation techniques feasible in the case study converter and their comparison with corresponding (baseline) full-bridge topology.

The comparison between topologies is application-agnostic and considers both uni- and bi-directional applications. The experimental results provided for PV applications are used to corroborate findings and demonstrate the performance of these PPCs in a real application. The paper is organized in the following manner. The existing and proposed current fed PPC topologies with their modulations are given in Section II. Section III discusses the comparative assessments of the current fed dc-dc PPC topologies. The experimental validation is provided in Section IV. Finally, Section V summarizes the results.

II. PPC Topologies and Modulations

The case-study S-PPC configurations employing CF dc-dc are demonstrated in Fig. 1, where Fig. 1(a) and (b) represent the full bridge high frequency-ink inverter (FB-HFLI) based and push-pull based PPC topologies, respectively. PV string at the input is used just as an application example, while these topologies are applicable across a wide range of uni- and bi-directional applications. In both cases, the input source is integrated in series with the SP along with a solid-state circuit breaker (SSCB), whereas the dc bus is connected to the parallel port (PP), i.e., the high-voltage side of the dc-dc stage. Both PPCs provide step-up/down voltage regulation as matrix switches enable polarity change in the SP. These PPCs differ in the switch count of the CF SP. In FB-HFLI, eight switches are arranged as a matrix inverter connected to a two-winding transformer, which enables bipolar voltage operation with bidirectional current capability. On the other hand, the CF push-pull based PPC employs only four switches and a three-winding transformer. This section elaborates on PPC configurations and their modulations for the forward power flow direction.

Protection in dc-coupled systems, such as dc microgrids, is often associated with the use of a DC circuit breaker, where solid-state solutions provide the ultimate speed of fault clearance [34]. Embedding an SSCB into the PPC instead of just connecting in series with a converter was suggested in [35], with examples of such implementation given in [36], [37], [38]. At the system level, this does not change the overall power losses but helps resolve the main drawbacks of the PPCs, such as soft start and protection, as discussed in [39].

In several emerging applications, like dc buildings, protection zones are defined along with particular protection requirements [40]. For example, the set of rules developed by the

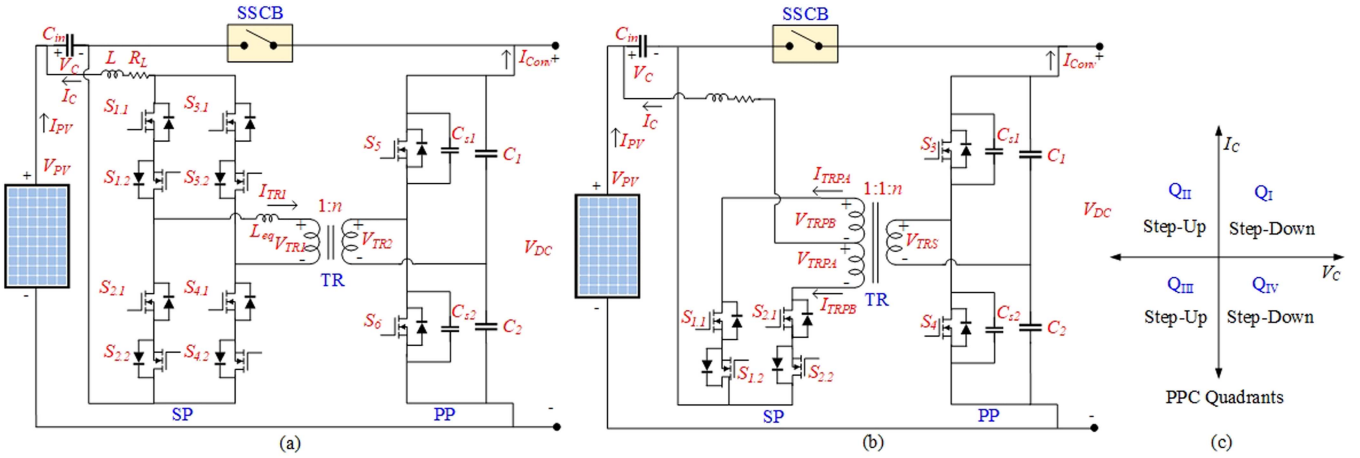

Fig. 1. PPC configurations with CF dc-dc: (a) Based on FB HFLI topology [32]; (b) its push-pull implementation; and (c) dc-dc operating quadrants.

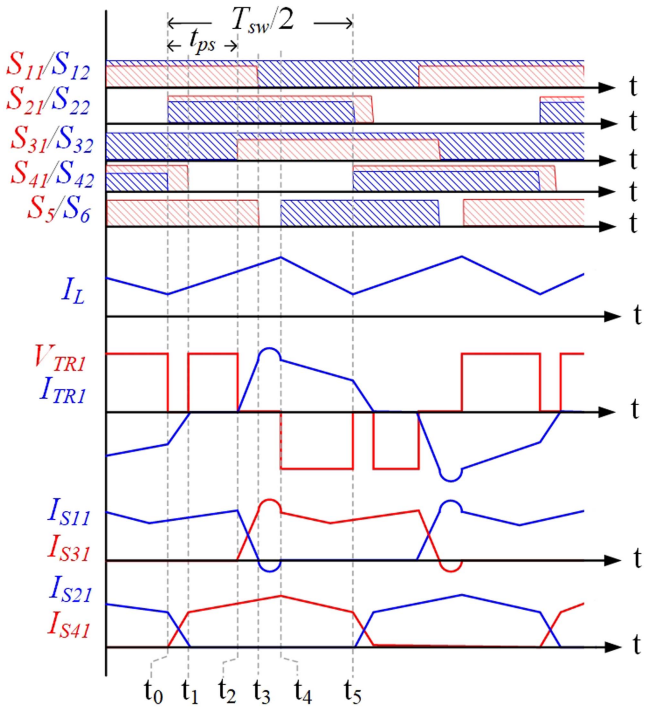

Fig. 2. Generalized waveforms for the conventional FB-HFLI based PPC.

industry-driven Current/OS Foundation suggests that residential stationary energy storage would fall under "Zone 3" [42], where semiconductor-based breakers corresponding to the forthcoming IEC60947-10 standard [41] must be used for protection. Moreover, embedded protection makes these PPCs potentially compliant with other application-specific safety standards requiring overcurrent protection, like IEC 60947-2 for electrical installations in buildings, US NEC Article 706 and IEC 62485-2:2018 for energy storage systems, US NEC Article 690 and IEC 62109-1:2010 for PV installations, and others similar regulations, without the need for external protection devices. The converter under study employs simple SSCB based on a series connection of two MOSFETs, which was designed according to [43].

A. Baseline PPC Based on FB-HFLI

1) Phase Shift Modulation – Fig. 2: With this modulation, the phase shift between the top and bottom side switches of the SP port (S_3-S_2 or S_1-S_4) controls the shoot-through state (t_1-t_2) and, consequently, the series port voltage and the input current. The energy transfer direction is from the SP to the PP. Hence, the dc-dc cell operates as a boost converter matching the SP voltage with the dc microgrid voltage. There is an overlap between SP switches to allow the current redistribution between top or bottom switches (t_0-t_1 and t_2-t_3) when one is turning on and the other is turning off (S_2-S_4 and S_1-S_3). This overlap must be long enough to allow the complete current redistribution. Thus, these switches can be turned off with ZCS.

The S_{12} and S_{32} are turned on continuously, while S_{22} and S_{42} work in synchronous rectification mode to prevent negative switch current when I_{S21} or I_{S41} reaches zero (at t_1, for ex.). There is also a constant phase shift between PP and SP switches (t_{ps}) and a dead time between PP switches to allow the completion of the resonance period (t_3-t_4). The resonance period ensures full charge/discharge of snubber capacitors (C_{S1}, C_{S2}) of the PP switches, resulting in power-independent ZVS turn-on of S_5 and S_6. The power circulation between both transformer ports is minimized as the winding voltage is zero during this resonance period. The dc voltage gain of the dc-dc stage is given in Table I.

2) Reverse Power Flow Control – Fig. 3: The voltage gain in the forward operation mode with PSM modulation is load-dependent. Hence, by keeping a constant current in the current source side, the dc-dc stage cannot boost the low SP voltage values to the dc microgrid voltage. Consequently, a dead zone (DZ) could be introduced to skip this critical operation zone in the PSM modulation ($V_C < V_{Th}$) [32]. Another solution is to implement a different modulation technique with a higher boost factor than the PSM. The switching and current-voltage waveforms of the converter with reverse power flow control modulation are depicted in Fig. 3. The shoot-through state duration (t_{ps}) alongside the reverse power flow interval (t_{rev}) controls the dc-dc stage voltage gain. All the converter switches

TABLE I
COMPARATIVE ASSESSMENT-I WITHIN CURRENT FED PPC TOPOLOGIES

Topology	Modulation	Feasible Voltage Regulation Range (ΔVC)	Mode Transition	Dead Zone	DC Voltage Gain	
					Forward Mode (Q_{IV})	Reverse Mode (Q_{III})
Current fed FB-HFLI [32]	PSM	±30 V	Forceful	Yes	$G_{FRW}=\frac{2\cdot\pi\cdot n}{1-\frac{2}{T_{SW}}\left(\frac{t_{PS}}{\pi}+\frac{2nL_{eq}(2I_{C(\max)}-I_C)}{V_{DC}}\right)}$	$G_{RV}=\frac{\pi-(t_{PS}+\omega\cdot t_{red})}{2\cdot\pi\cdot n}$
Current fed FB-HFLI [26], [32]	PSM +t_{rev}	±30 V	Seamless	Yes (Operable)	During Non-Dead Zone: $G_{FRW}=\frac{2\cdot\pi\cdot n}{1-\frac{2}{T_{SW}}\left(\frac{t_{PS}}{\pi}+\frac{2nL_{eq}(2I_{C(\max)}-I_C)}{V_{DC}}\right)}$; During Dead Zone: $G_{FRW}=\frac{2\cdot n}{1-t_{PS}-2\cdot t_{rev}}$	
Current fed push-pull PPC [33]	t_{rev}	±50 V	Seamless	No	$G_{FRW}=\frac{V_{DC}}{2nV_C}=\frac{1}{1-2.t_{rev}}$	$G_{RV}=\frac{2nV_C}{V_{DC}}=1-2.t_{rev}$
Proposed current fed resonant push-pull PPC	t_{rev} + Resonance	±50 V	Seamless	No		

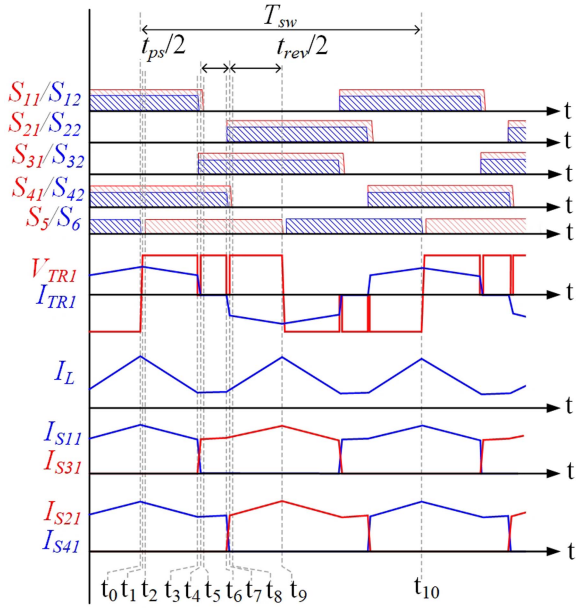

Fig. 3. Generalized waveforms for FB-HFLI reverse power flow modulation.

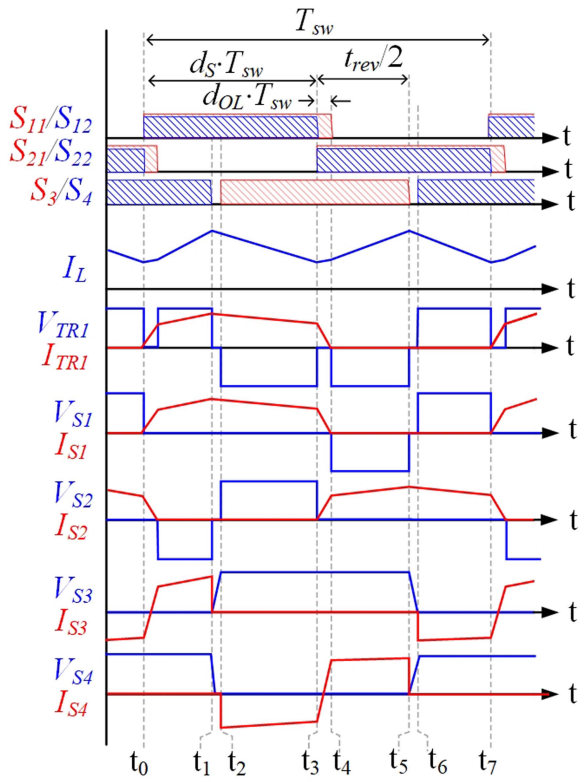

Fig. 4. Generalized waveforms for the conventional CF push-pull based PPC.

work in the soft switching mode, ensured by the overlap time in the SP side switches and dead time in the PP side switches. It allows for ZCS turn-off of SP side switches and ZVS turn-on of PP side switches. More details on this modulation are given in [19].

The dc voltage gain for this modulation is given in Table I. Usually, the reverse power flow, i.e., circulating energy, is avoided in the power electronic converters. Here, it is utilized in a narrow voltage range (DZ) near zero SP voltage to extend the boost factor of the dc-dc stage. Hence, the impact of the reverse power flow on the PPC efficiency is negligible. In practice, both t_{rev} and t_{ps} are used to achieve high dc voltage gain, where t_{rev} control provides a wider voltage regulation range as the voltage gain is more sensitive to this parameter.

B. Current Fed Push-Pull Dc-Dc PPC

1) Conventional Modulation – Fig. 4: The modulation sequences and the current-voltage waveforms of the push-pull converter with the conventional modulation are illustrated in Fig. 4. Similar to the FB-HFLI converter, the energy transfer from the SP to the PP is controlled by the reverse power flow interval needed to store the energy in the inductor (t_3-t_5). The SP side switches redistribute their current when one turns on

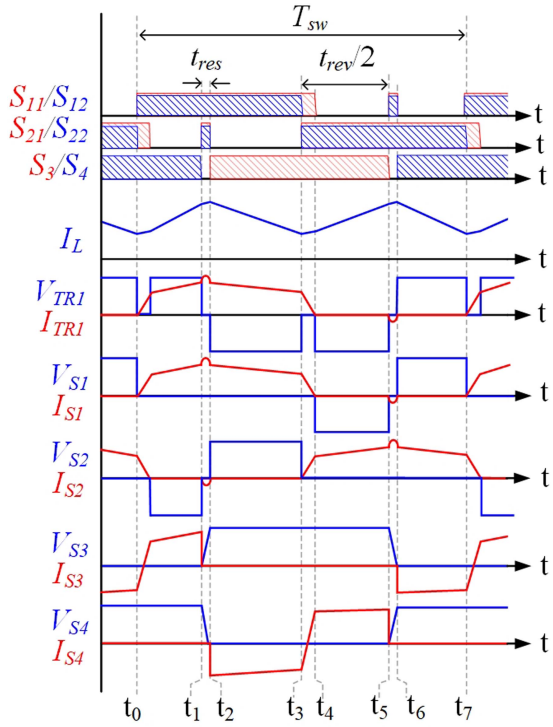

Fig. 5. Generalized waveforms for the proposed quasi-resonant modulation.

and the other turns off (S_1 and S_2) with ZCS. Switches S_{12} and S_{22} work with a 50% duty cycle to provide synchronous rectification within four-quadrant switches S_1 and S_2 to avoid the negative current values and turn them off with ZCS (t_3-t_4). The soft turn-on of the SP side switches is fulfilled by the leakage inductance of the transformer, which decreases the *di/dt* in switches. On the other hand, PP side switches have dead time to fulfill the charge/discharge of their snubber capacitor, needed for ZVS turn-on and off. In practice, the full ZVS cannot be implemented solely by the snubber capacitor. In fact, the snubber capacitors decrease the *dv/dt* in PP switches, reducing the switching losses compared to the total hard switching (t_1-t_2) [19]. A simplified voltage gain of the converter in forward mode is stated in Table I, in which t_{rev} is the reverse power flow state duty cycle.

2) Resonant-State Modulation – Fig. 5: To avoid switching losses in PP side switches and achieve complete ZVS, a new modulation strategy (Fig. 5) is proposed in this paper. It differs from the conventional modulation in a resonance period introduced to accelerate the charge/discharge time of PP side snubber capacitors. The resonant process provides enough energy to complete the charge and discharge of these capacitors even at zero operating power. This process happens during (t_1-t_2) and (t_5-t_6) in each switching cycle with a period of T_{SW}. By turning on both SP side switches, the leakage inductance of the SP side of the transformer is short-circuited, creating a resonance circuit with snubber capacitors of the PP side switches. To fulfill ZVS criteria, the accumulated energy inside the leakage inductance must exceed the energy of snubber capacitors to fully charge/discharge them and turn on the PP side switch in ZVS condition. The voltage gain of the converter is similar to the conventional modulation.

III. Comparative Assessment

As discussed, PPC offers different performances with different modulations for the same application. It is essential to perform a comparative assessment between the PPCs to identify the topology and modulation with superior performance. Since a DAB-based PPC has step-up/down capability along with bidirectional power flow, this makes it the closest competitor of the FB-HFLI-based PPC. On the other hand, the DAB-based PPC suffers from poor performance close to zero partiality, as follows from a detailed comparison between FB-HFLI and DAB-based PPCs represented in [26]. Therefore, a detailed comparative study is done for current fed FB-HFLI and push-pull based PPCs with various modulations elaborated in Tables I–III. It is worth mentioning that the comparison has been made for the same operating conditions and did not target any specific application for generalization.

It should be noted that Table II provides the data about the dc-dc stage associated with the PPC. It can be observed that the current fed FB-HFLI [26] incorporates a total of 10 semiconductor switches (SP: 8, PP: 2), while the push-pull configuration comprises only 6 switches (SP: 4, PP: 2). This significant difference gives the substantial variance in the PPC efficiency (η_{PPC}). This happened mainly because of the switch power loss of the semiconductor devices (S_1-S_6). The switch power loss (P_{Switch}) consists of conduction loss (P_{Con}), switching loss (P_{Sw}), reverse recovery loss (P_{rr}) and loss due to output capacitance (P_{Coss}). It is generalized in Table II that the FB-HFLI topology features higher P_{Switch} from the higher number of switches on the SP side. The transformer loss (P_{TR}) consists of the core loss and winding loss. At the same time, inductor losses (P_L) include loss due to ac resistance and dc resistance. These P_{TR} and P_L can be calculated based on the measurement of actual parasitic parameters or using datasheet information. The loss associated with solid-state circuit breaker (P_{SSCB}) occurs due to the conduction of SSCB. Here, P_{rest} defines the remaining losses associated with the consumption of auxiliary power supply, parasitic conductions losses, and loss prediction errors arising from a wide allowed variation range of MOSFETs' parameters. Table II provides the generalized expressions for loss calculation.

The switches with $R_{DS(on)}$ of 60 mΩ and 120 mΩ were used in the SP and PP sides, respectively, and 75 mΩ in SSCB. The losses were calculated for $V_{DS(max)}$, $I_{DS(RMS)}$ = 150 V, 4.6 A and 400 V, 2.5 A, respectively, for FB-HFLI and push-pull based PPCs, based on experimental measurements and theoretical calculations. Hence, the calculated distribution of losses is illustrated in Fig. 6. It is evident that the push-pull topology offers fewer conduction losses. As the conventional modulation provided limited soft switching, some switching losses are still present because of partial hard switching. As discussed in Section II, the proposed modulation for push-pull PPC improves

TABLE II
COMPARATIVE ASSESSMENT-II WITHIN THE CURRENT FED DC-DC STAGE

Topology	Associated components				SP switch SS stress	Soft switching	Semiconductor power losses	
	Switch	Inductor	Capacitor	Transformer			Conduction	Switching
Current fed FB-HFLI [19], [20]	10	1	2	Two windings	V_{Sw}	Full ZVS, ZCS	$P_{Contotal}=10\times R_{DS(on)}I_{DS}^2$	SP side $P_{Sw}=8\times\frac{1}{2}V_{DS}I_{DS}(t_{feff}+t_{reff})f_{Sw}$ $P_{Coss}=8\times\frac{1}{2}V_{DS}^2C_{oss}f_{Sw}$ $P_{rr}=4\times f_{sw}V_{DS}Q_{rr}$ $t_{feff}\approx 1.1$ ns, $t_{reff}\approx 1.1$ ns PP side $P_{Sw}=2\times\frac{1}{2}V_{DS}I_{DS}(t_{feff}+t_{reff})f_{Sw}$ $P_{rr}=2\times f_{sw}V_{DS}Q_{rr}$ $t_{feff}\approx 1.1$ ns, $t_{reff}\approx 1.1$ ns
Current fed push-pull PPC [23], [33]	6	1	2	Three windings	$2V_{Sw}$	Partially ZVS, ZCS	$P_{Contotal}=6\times R_{DS(on)}I_{DS}^2$	SP side $P_{Sw}=6\times\frac{1}{2}V_{DS}I_{DS}(t_{feff}+t_{reff})f_{Sw}$ $P_{Coss}=6\times\frac{1}{2}V_{DS}^2C_{oss}f_{Sw}$ $P_{rr}=2\times f_{sw}V_{DS}Q_{rr}$ $t_{feff}\approx 12$ ns, $t_{reff}\approx 12$ ns PP side $P_{Sw}=6\times\frac{1}{2}V_{DS}I_{DS}(t_{feff}+t_{reff})f_{Sw}$ $P_{rr}=2\times f_{sw}V_{DS}Q_{rr}$ $t_{feff}\approx 12$ ns, $t_{reff}\approx 12$ ns
Proposed current fed resonant push-pull PPC	6	1	2	Three windings	$2V_{Sw}$	Full ZVS, ZCS	$P_{Contotal}=6\times R_{DS(on)}I_{DS}^2$	SP side $P_{Sw}=6\times\frac{1}{2}V_{DS}I_{DS}(t_{feff}+t_{reff})f_{Sw}$ $P_{Coss}=6\times\frac{1}{2}V_{DS}^2C_{oss}f_{Sw}$ $P_{rr}=2\times f_{sw}V_{DS}Q_{rr}$ $t_{feff}\approx 1.1$ ns, $t_{reff}\approx 1.1$ ns PP side $P_{Sw}=6\times\frac{1}{2}V_{DS}I_{DS}(t_{feff}+t_{reff})f_{Sw}$ $P_{rr}=2\times f_{sw}V_{DS}Q_{rr}$ $t_{feff}\approx 1.1$ ns, $t_{reff}\approx 1.1$ ns

SS-Steady State, t_{feff} – effective fall time, t_{reff} – effective rise time

this by integrating an additional resonant interval. In Fig. 6, it can also be noticed that the P_{Sw} in push- pull based PPC with the proposed modulation is negligible. Consequently, the proposed current fed push-pull PPC with quasi-resonant modulation offers excellent PPC efficiency.

Since P_{Con} dominates switch power losses, η_{PPC} can be improved by selecting high-end semiconductor devices with low $R_{DS(on)}$. The best feasible case is calculated based on the devices available on the market, namely, $R_{DS(on)}=7.5$ mΩ for both dc-dc sides. Fig. 7 represents the corresponding power loss breakdown, while other parameters are kept the same. The important point is that the low-$R_{DS(on)}$ devices are costly, and a trade-off between cost and efficiency needs to be found.

Every component cost is assessed concerning the cost of the same kind of component used in the current fed FB-HFLI because the absolute costs of the components are influenced by various factors, including the nominal productions of the manufacturing company, the location of the manufacturing site, the availability of raw material suppliers, the cost of transportation, and market price fluctuations and uncertainties [44]. Table III compares the relative cost, power density, component stress factors, and control complexity between FB-HFLI and push-pull PPC. An example of an efficiency-optimized full power dc-dc converter from [46] was introduced to demonstrate extreme optimization with paralleling of switches (2 devices per switch at the input and 11 devices per switch at the output). It could be observed that PPC can provide sizable cost reduction compared

TABLE III
COMPARATIVE ASSESSMENT WITHIN CURRENT FED PPC TOPOLOGIES

Topology	Switch			Capacitor			Total price (€)	Control Complexity	Power Density (kW/liter)
	Count	Unit price (€)	Sum (€)	Count	Unit price (€)	Sum (€)			
Current fed FB-HFLI [32]	SP:2	11.45	22.9	C_{in}:1	21.20	21.20	137.72	High	1.23*
	PP:8	9.43	75.44	$C_{1\text{-}2}$:2	9.09	18.18			
Current fed FB-HFLI [26], [32]	SP:2	11.45	22.9	C_{in}:1	21.20	21.20	137.72	High	
	PP:8	9.43	75.44	$C_{1\text{-}2}$:2	9.09	18.18			
Current fed push-pull PPC [33]	SP:2	11.45	22.9	C_{in}:1	21.20	21.20	100	Moderate	
	PP:4	9.43	37.72	$C_{1\text{-}2}$:2	9.09	18.18			
Proposed current fed resonant push-pull PPC	SP:2	11.45	22.9	C_{in}:1	21.20	21.20	100	Moderate	
	PP:4	9.43	37.72	$C_{1\text{-}2}$:2	9.09	18.18			
Efficiency-optimized DAB converter [46]	In: 8	13.80	110.40	C_{Out}: 44	1.18	51.92	340.74	High	2.3
	Out: 22	8.11	178.42						

*Preliminary design optimization demonstrates the potential to increase power density to 4 kW/liter.
SP: G3R60MT07D, PP: C3M0120090J, C_{in}: EZP-V60107MTC, $C_{1\text{-}2}$: B32778Z8606K000,
In: IPW60R041C6, Out: IRFP4668PBF, C_{out}: GCJ32DR72A225KA01K

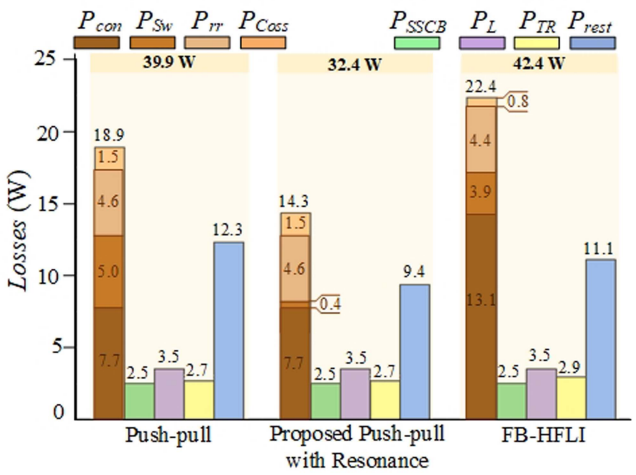

Fig. 6. Power loss breakdown for three PPC configurations at 2.5 kW for V_{DC} = 350 V and V_C = 30 V.

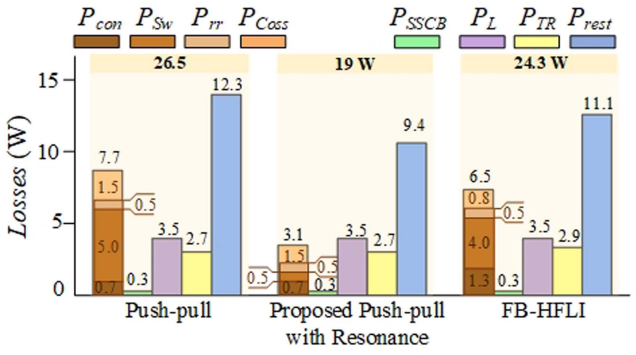

Fig. 7. Power loss breakdown for three PPC configurations at 2.5kW for V_{DC} = 350 V and V_C = 30 V using high-end semiconductors.

to the full power converter of comparable efficiency. It is worth noting that the prototype built for this study aimed at verifying analytical loss models while further optimization for efficiency and power density is possible and will be addressed in future

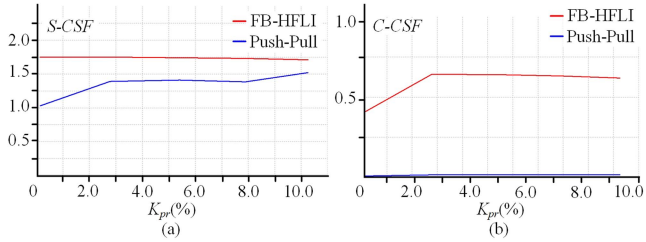

Fig. 8. CSFs of FB-HFLI and CF push-pull based PPC evaluated for (a) switches and (b) capacitors.

studies. It was assessed that the power density could be tripled, pending practical verification, while the full power converter from [46] was built in favor of efficiency and power density and has limited room for further improvements. The cost difference between PPC and full power converter would be even higher if the substantial cooling system of the latter is taken into account.

In [15], a component stress factor (CSF) calculation is provided. The switch CSF (S-CSF) for switching devices is calculated by multiplying its maximum blocking voltage (V_{Smax}) by the corresponding root mean square current (I_{Crms}) as given in (1). Similarly, the capacitor CSF (C-CSF) is also evaluated by the multiplication of maximum voltage (V_{Cmax}) to the rms current as stated in (2). Fig. 8 illustrates a comparison of S-CSF and C-CSF for FB-HFLI and push-pull-based PPCs.

$$\mathrm{S-CSF} = \sum_i \frac{V_{Smax}^2 \cdot I_{rms}^2}{P_{rated}^2} \tag{1}$$

$$\mathrm{C-CSF} = \sum_i \frac{V_{Cmax}^2 \cdot I_{Crms}^2}{P_{rated}^2}. \tag{2}$$

On the other hand, the push-pull configuration features twice the voltage stress of the SP switches compared to that of the FB-HFLI topology, which is a typical drawback. Table IV illustrates an evaluation of switch stresses among the configurations. Therefore, it can be summarized that PPCs have higher efficiency than conventional full-power converters, η_{PPC} can be

TABLE IV
EXPERIMENTAL SWITCH STRESSES OF CURRENT FED DC-DC BASED PPCS

At 2kW, V_{PV}=320 V, V_{DC}=350 V								
Topology	PP Switch stress				SP Switch stress			
	Voltage (V)		Current (A)		Voltage (V)		Current (A)	
	$\hat{V}_S$	$\hat{V}_S$	I_S	$\hat{I}_S$	$\hat{V}_S$	$\hat{V}_S$	I_S	$\hat{I}_S$
FB-HFLI [19]	350	380	2.4	24	75	85	3.5	5.5
Push-pull [33]	350	391	2.8	11.2	220	339	4.9	11.2
Proposed push-pull (PP)	350	391	2	5	192	328	4.9	11.2
At 2kW, V_{PV}=350 V, V_{DC}=350 V								
Topol	PP Switch stress				SP Switch losses			
	Voltage (V)		Current (A)		Voltage (V)		Current (A)	
	$\hat{V}_S$	$\hat{V}_S$	I_S	$\hat{I}_S$	$\hat{V}_S$	$\hat{V}_S$	I_S	$\hat{I}_S$
FB-HFLI [19]	350	380	2.4	9.6	75	85	3.6	5.25
Push-pull [33]	350	391	2.8	11.2	217	336	4.6	11.2
Proposed PP	350	391	1.9	5.6	197	332	4.8	11.2
At 2kW, V_{PV}=380 V, V_{DC}=350 V								
Topology	PP Switch stress				SP Switch losses			
	Voltage (V)		Current (A)		Voltage (V)		Current (A)	
	$\hat{V}_S$	$\hat{V}_S$	I_S	$\hat{I}_S$	$\hat{V}_S$	$\hat{V}_S$	I_S	$\hat{I}_S$
FB-HFLI [19]	350	380	1.12	2.3	75	85	3.7	7.5
Push-pull [33]	350	391	2.75	11.2	225	348	4.1	11.2
Proposed PP	350	391	1.9	5.6	196	326	4.2	11.2

increased further to more than 99.6% by selecting proper devices and best-performing modulation.

The isolation TR, a crucial part of the PPC, determines the voltage regulation range. The CSF of the PPC in the given architecture is lowered by decreasing the leakage inductance (L_{eq}) of the TR. The reduced L_{eq} also reduces the duty cycle loss and resonance intervals. Therefore, selecting the least L_{eq} can significantly reduce the power circulation during the resonance period [19]. The value of the minimum turns ratio (n_{min}), which is generally stated as (3), is determined by the minimum battery voltage. Equation (4) can be used to calculate the TR's maximum flux density ($B_{\max}$).

$$n_{\min} = \frac{V_{dcmin}}{2 \cdot t_{ps} \cdot V_{Cmax}} = \frac{V_{dcmin}}{2 \cdot t_{ps} \cdot (V_{dcmin} - V_{PVmax})} \quad (3)$$

$$B_{\max} = \frac{V_{dcmin}}{4 \cdot n_p \cdot f_{sw} \cdot A_e} \quad (4)$$

where A_e and n_p represent the effective cross-section of the HFT core and the number of turns on the SP side. The design demonstrated in Fig. 9 ensures the lowest possible leakage inductance. Nevertheless, the small leakage inductance cannot be neglected. Hence, all the prototypes in this study employed a simple regenerative passive snubber from [45].

IV. EXPERIMENTAL RESULTS

A prototype depicted in Fig. 10 was designed to evaluate case-study PPC configurations. The detailed specifications of the experimental setup are given in Table V. To emulate a

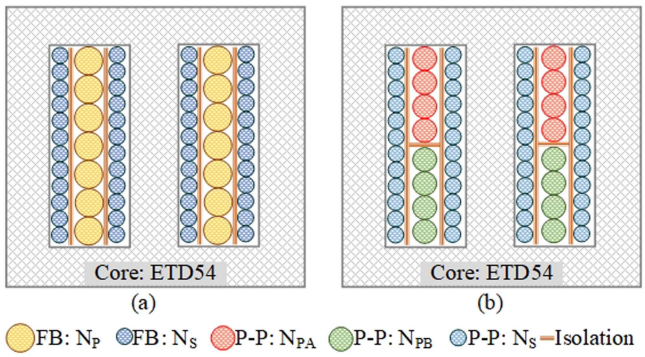

Fig. 9. HFT winding arrangements for (a) full-bridge and (b) push-pull.

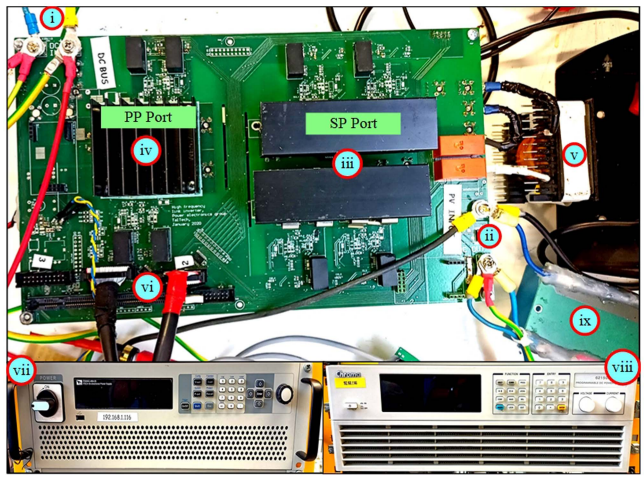

Fig. 10. Experimental prototype of PPC and power supplies used: (i) Dc bus terminal; (ii) PV terminal; (iii) series port switches with heat sinks; (iv) parallel port switches with heat sinks; (v) filter inductor; (vi) controller signals; (vii) dc power source; (viii) PV emulator; (ix) input capacitor.

TABLE V
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Symbol	Value
dc bus voltage	V_{dc}	350 V
Filter inductor	L	100 µH
Transformer primary side leakage inductance and ESR	L_{eq1}, R_{eq1}	2µH 82 mΩ
Transformer secondary side leakage inductance and ESR	L_{eq2}, R_{eq2}	0.6 µH 46 mΩ
Transformer tertiary side leakage inductance and ESR	L_{eq3}, R_{eq3}	0.5 µH 49 mΩ
magnetizing inductance	L_m	2.5 mH
Transformer ratio	1:1:n	1:1:2
Half-bridge capacitors	C_1 and C_2	66 µF
Snubber capacitors	C_{s1} and C_{s2}	1.1 nF
Series Capacitor	C_{in}	100 µF
Maximum PV power Maximum PV voltage Maximum PV current	P_{PVMP} V_{PVMP} I_{PVMP}	2.2 kW 320 V to 380 V 6 A
Switching frequency	f_s	50 kHz
Ambient Temperature	$Temp$	10° C to 45° C

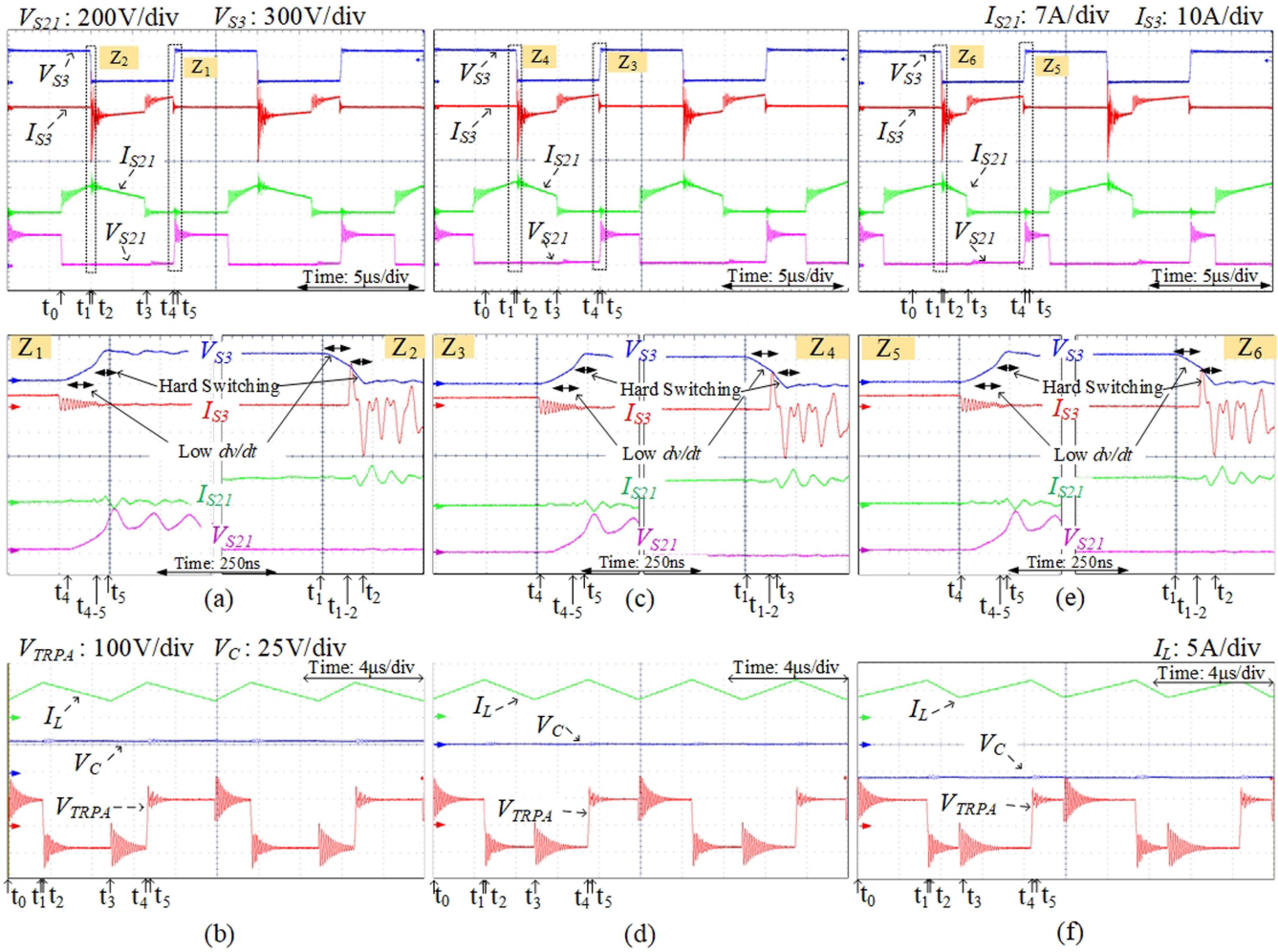

Fig. 11. Operation of conventional push-pull PPC. Switching characteristics of SP switch S_{11}, PP switch S_4 at $P_{PV} = 2$ kW and $V_{DC} = 350$ V while (a) $V_{PV} = 380$ V and $V_C > 0$, (c) $V_{PV} = 350$ V and $V_C = 0$, i.e., DZ, and (e) $V_{PV} = 320$ V and $V_C < 0$, along with and key waveforms of magnetic components in (b), (d), and (f).

photovoltaic (PV) string consisting of ten conventional 60-cell monocrystalline PV modules, a PV simulator Chroma 62150H-1000S is employed. This simulator can generate PV profiles while introducing variations in ambient temperature. Moreover, it allows for real-time monitoring and logging of various crucial parameters, including V_{PV}, I_{PV}, P_{PV}, and MPPT efficiency (η_{MPPT}) as presented in the experimental results. The dc bus is implemented using a bi-directional DC power supply iTECH IT6006C-800-25. Within the power stage of the PPC prototype, SiC MOSFETs (120 mΩ/900 V) and (60 mΩ/600 V) are used in the SP and PP, respectively.

This choice ensured the safety of the prototype during testing, especially in critical operating modes. The SP and PP components are interconnected via a high-frequency transformer. The SP section was equipped with a filter inductor and an input capacitor to enhance performance. This setup was used to obtain RMS and peak (denoted with ^) voltage/current stress values in Table IV.

In the control stage, an STM32G474 control board is used. It aggregates voltage and current data from sensors and generates modulation signals for controlling the switches in SP and PP. To assess the efficiency of the PPCs, the measurements are conducted using a Yokogawa WT1800E power analyzer with ±0.05% basic accuracy. The following results provide a comparative assessment of push-pull PPC with different modulations and a comparison with the baseline FB-HFLI topology. Another case study is carried out for push-pull PPC interfacing a PV string to evaluate its efficiency η_{PPC} and MPPT efficiency η_{MPPT}.

A. Performance of CF Push-Pull Based PPC

The performance of single inductor push-pull PPC (as shown in Fig. 1(b) is evaluated with conventional modulation (refer to Fig. 3). Fig. 11 illustrates the currents and voltage transients of SP and PP side switches S_{21} and S_3, respectively, for all three modes which are $V_C > 0$, $V_C = 0$, and $V_C < 0$. The step-up/down operation is demonstrated at $P_{PV} = 2.5$ kW, $V_{DC} = 350$ V, and $V_{PV} = \{320\text{ V}, 350\text{ V}, 380\text{ V}\}$. In Fig. 11(a)–(c), at the instant t_0, S_{21} and S_{22} turn on with ZVS assisted by transformer leakage inductance. At t_1, the PP switches change their switching state

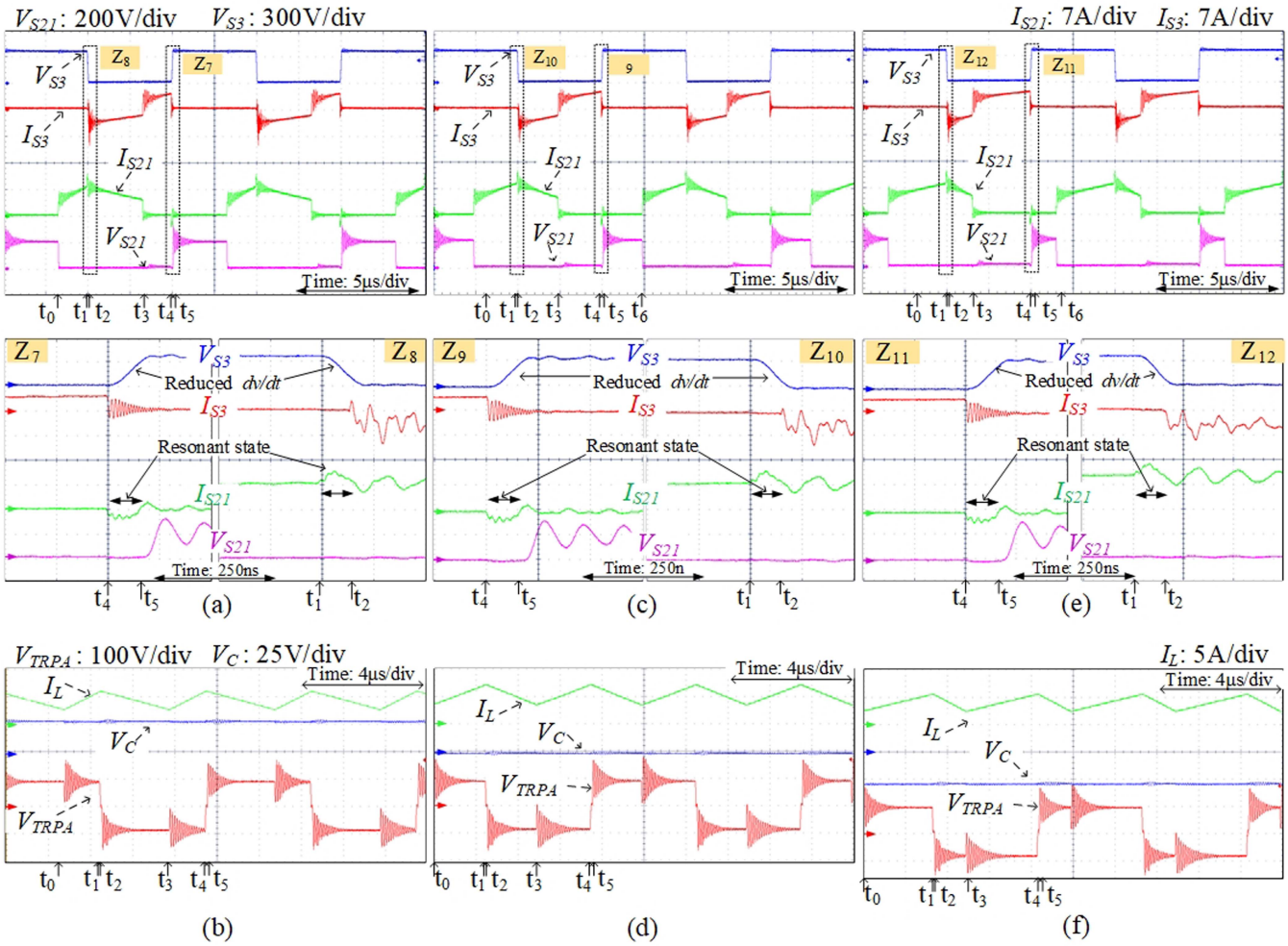

Fig. 12. Operation of proposed resonant push-pull PPC. Switching characteristics of SP switch S_{11}, PP switch S_4 at $P_{PV} = 2$ kW and $V_{DC} = 350$ V while (a) $V_{PV} = 380$ V, i.e., $V_C > 0$, (c) $V_{PV} = 350$ V, i.e., $V_C = 0$ or DZ, and (e) $V_{PV} = 320$ V, i.e., $V_C < 0$ along with and key waveforms (b), (d), and (f), respectively.

accordingly. As the switch S_3 turns on, V_{S3} rises to an amplitude value while I_{S3} falls.

Here, the ZVS (minor *dv/dt*) supported by snubber capacitor till $t_{1\text{-}2}$ can be seen in zoomed sections Z_2, Z_4, and Z_6. This *dv/dt* also exists during t_4 to $t_{4\text{-}5}$, as Z_1, Z_3, and Z_5 show. Moreover, intervals from $t_{1\text{-}2}$-t_3 and $t_{4\text{-}5}$-t_5 feature partial hard switching, leading to losses. The same switching process happens to S_4 also. Next to t_3, S_{21} and S_{22} start to turn off. At t_4, S_3 begins to turn off with ZCS, V_{S3} starts to fall down, while I_{S3} rises again. Here, the partial soft switching during the turn-off of S_3 can be noticed. Fig. 11(b), (d), and (f) exhibit the transformer voltage (V_{TRPA}), filter inductor current (I_L), and differential voltage (V_C) for all three modes.

B. Performance of the PPC Based on the CF Push-Pull With Quasi-Resonant Modulation

It has been demonstrated that the snubber capacitors in push-pull PPC cannot provide complete soft switching, leading to unavoidable losses in the PP switches. This issue can be improved by integrating an additional resonant state along with conventional modulation (refer Fig. 5). The demonstrations of the proposed resonant push-pull PPC are shown in Fig. 12. This study is performed with the same constraints at $P_{PV} = 2.5$ kW, $V_{dc} = 350$ V, and V_{PV} of 320 V, 350 V, and 380 V. Sub Fig. 12(a), (c), and (e) illustrate the switching processes of the SP switches S_{21} and S_{22} and PP switch S_3. The resonant state can be observed in the intervals t_1-t_2 and t_4-t_5. Due to this, a bump is presented in the I_{21} and I_{S22} as shown in the zoomed sections Z_7-Z_{12}. This resonant state helps to ensure low *dv/dt* of switches S_3 and S_4 during turning on and off, which results in complete soft switching.

Here, intervals t_1-t_2 and t_4-t_5 represent the ZVS turn-on and -off of the PP switch S_3. ZVS of S_3 can be seen in the zoomed sections.

Due to the soft switching, the η_{PPC} increases by a sizable amount, which can be seen in the next subsections. Corresponding V_{TRPA}, I_L and V_C are shown in Sub Fig. 12(b), (d), and (f) for three PV string voltages. Table VI comprises all control parameters associated with the SP and PP switches corresponding to the figures. An η_{PPC} curve at different power levels is exhibited in Fig. 13(a) for both FB-HFLI and push-pull PPCs.

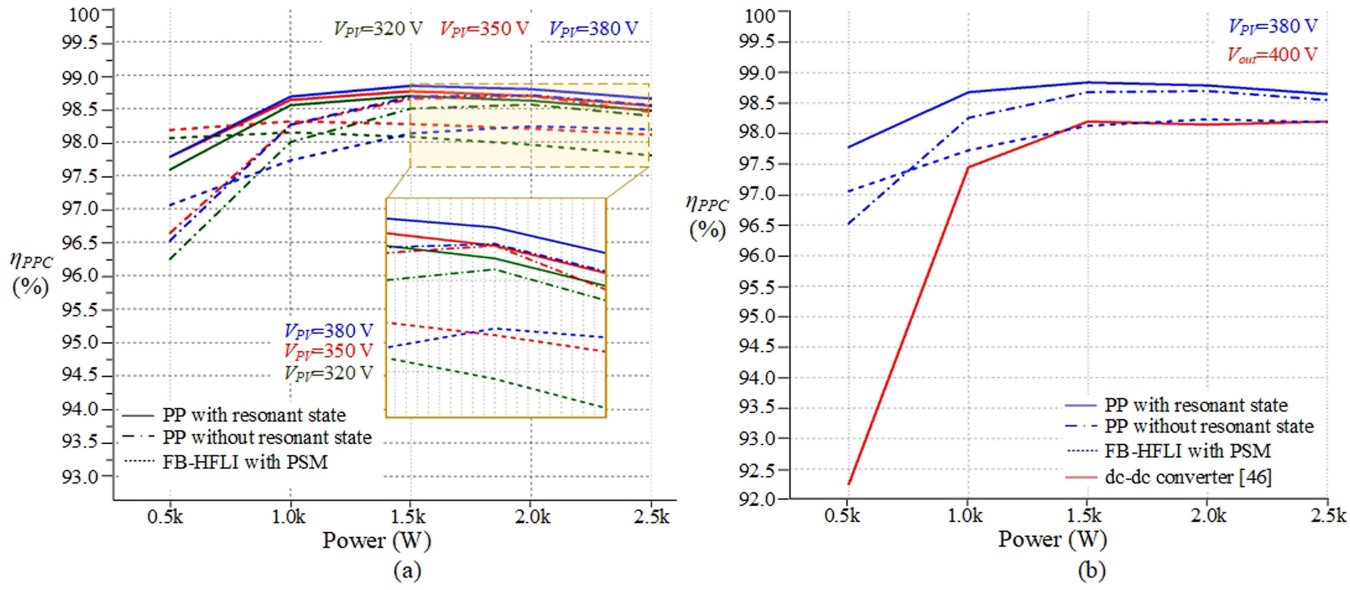

Fig. 13. Efficiency curves: (a) The case study PPC implementation at different power and voltage levels and (b) the full power dc-dc converter [46] compared to the studied PPCs.

TABLE VI
DUTY CYCLES, OVERLAP PERIOD, RESONANT PERIOD, AND POWER CONTROL PARAMETER

SP Switches			PP Switches		
d_{S11} & d_{S21}	d_{S12} & d_{S22}	d_{OL}	d_{S3} & d_{S4}		t_{res}
0.5	0.53	0.03	0.492	0.492	0.8%

Figures	Fig. 11			Fig. 12		
	(a)	(c)	(e)	(a)	(c)	(d)
t_{rev}	0.17	0.25	0.33	0.16	0.25	0.34

It clearly shows the enhanced performance of the proposed resonant push-pull topology with the utmost η_{PPC}.

The efficiency of the PPCs could be compared to that of the high-end implementations of full power dc-dc converters, as shown in Fig. 13(b). Highly optimized full power dc-dc converter is similar in efficiency to non-optimized HFLI-based PPC at full power, while its efficiency deteriorates at light load. The PPC based on the CF push-pull with resonant state demonstrates the best efficiency of them all. This proves the initial hypothesis that PPC based on CF push-pull topologies can provide better performance than those based on more widely used CF full-bridge topologies.

C. Performance of the FB-HFLI-Based PPC in PV String Applications

This case study describes how standard modulation of the FB-HFLI topology has limitations since it stops the PPC from switching quadrants during quadrant transitions. The MPPT performance of PPC with a traditional modulation is shown in Fig. 14. Throughout the operation, V_{dc} is kept at 350 V. The process begins with step-down mode (quadrant Q_{IV}), with PV cell temperature (*Temp*) set to 10 °C and $V_C \gg 0$. In the steady state, the PPC delivers 2.2 kW of its maximum power to the dc bus. At t_0, the *Temp* starts to rise, the voltage of the maximum

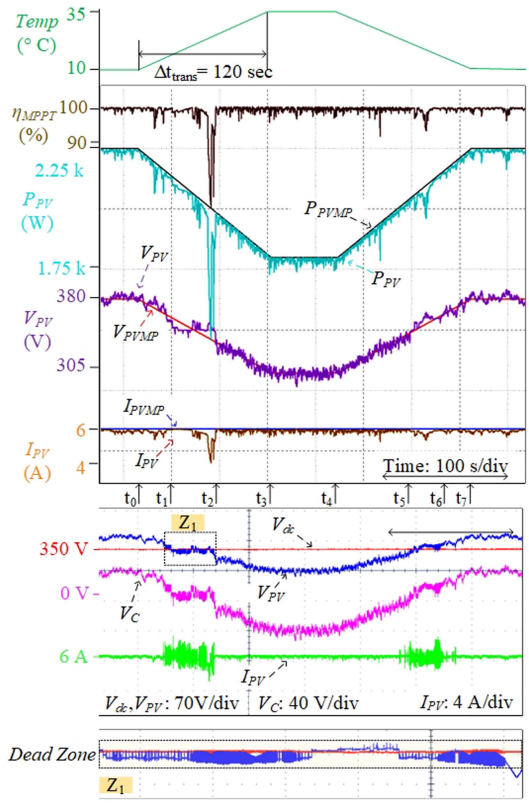

Fig. 14. The MPPT performance of the FB-HFLI-based PPC during PV cell temperature changes between 10 °C↔35 °C at V_{dc} = 350 V.

power point (MPP) V_{PV} starts to fall gradually, and the V_C also starts to decrease. The linear controller saturates when V_C reaches the DZ, i.e., $V_C = V_{Th}$ at the instant t_1. Here, V_{Th} is the maximum V_C when DZ starts. Hence, the PPC is forced to shift

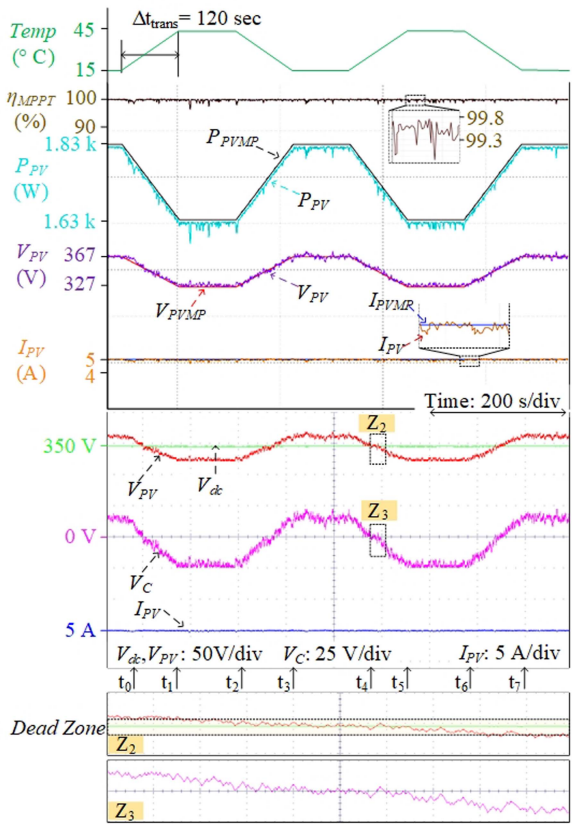

Fig. 15. The MPPT performance of the proposed push-pull PPC with quasi-resonant modulation during PV cell temperature changes between 15 °C↔45 °C at $V_{dc} = 350$ V.

its quadrants to Q_{III}. As the quadrants shift, PPC switches to step-up mode and searches for a feasible operating point closest to the MPP. The dead zone period remains till t_2. At t_3, the *Temp* stabilizes at 35 °C with $V_C \ll 0$, and PPC draws only 1.75 kW of power from the emulated PV string till t_4. Then, the PV cell temperature gradually increases to its initial value. Therefore, intervals t_4-t_5, t_5-t_6, and t_6-t_7 are defined as quadrant Q_{III}, dead zone, and quadrant Q_{IV}, respectively.

From these results, it can be concluded that a linear controller cannot switch the operating quadrant of a PPC smoothly. It requires an additional control subroutine that forcefully changes the operating quadrant of a PPC [32]. However, the dead zone is always present with this modulation. This issue can be solved by using push-pull PPC with the proposed quasi-resonant modulation within PPC to achieve seamless transitions between operating quadrants.

D. Performance of the CF Push-Pull Based PPC With the Quasi-Resonant Modulation in PV String Applications

In this case study, a performance study of the proposed quasi-resonant push-pull modulation is carried out for varying PV cell temperature. This variation of temperature provides the range of V_{PV} from 325 V to 375 V, which results in PPC operation in both quadrants (Q_{IV} and Q_{III}, see Fig. 1(c)). Fig. 15 represents parameters such as V_{PV}, I_{PV}, V_{dc}, V_C, and *Temp* for MPPT performance of quasi-resonant push-pull based PPC. Before t_0, the *Temp* is constant at 10 °C, resulting in $V_{PV} \gg V_{dc}$ and $V_C \gg 0$. The V_{dc} is maintained at 350 V throughout the entire operation. This results in the PPC operation in Q_{III}, also known as step-up mode. At t_0, *Temp* starts to rise, and V_{PV} starts to fall correspondingly. Since this dc-dc topology with this modulation allows the linear controller to change the PPC quadrants as the V_C becomes negative, $V_C << 0$ (at t_1), the PPC changes its mode of operation from step-up to step-down seamlessly by changing its quadrants from Q_{III} to Q_{IV}, respectively.

As the *Temp* settled back at 40 °C at t_2, the V_{PV} became 325 V, and the PPC extracts the maximum power of 1.33 kW. In the interval from t_2 to t_3, the operation continues in Q_{IV}. At t_3, *Temp* starts to fall down till t_5, which results in the increase in V_{PV} to 375 V. During this period, the PPC operates at a power of 1.83 kW. Between t_3-t_5, at t_4, the PPC changes its operating quadrant from Q_{IV} to Q_{III} without any disruption as the V_C smoothly changes its polarity from negative to positive. Thus, the experimental study proves that PPCs based on the proposed quasi-resonant CF push-pull do not feature a voltage DZ. It can smoothly change its operating quadrant, resulting in higher η_{PPC} and η_{MPPT} compared to FB-HFLI topology.

V. Conclusion

This paper studied and compared two PPCs based on current-fed full bridge and push-pull dc-dc topologies. The obtained results prove that modulation of dc-dc stage defines the performance of the corresponding PPC. With the help of several comparative assessments presented in the paper, it has been proven that the push-pull configuration has enhanced converter efficiency compared to the full bridge counterpart. Moreover, the smaller number of semiconductor devices opens opportunities for implementation cost reduction.

This paper proposes a quasi-resonant modulation for CF push-pull based PPC, which enhances its efficiency by over 1%, eliminating the switching losses present with the conventional modulation. A resonant interval was introduced in the switching sequence to enable power-independent soft-switching of the switches in the parallel port. The above claims are corroborated through the experimental tests by emulating PPC operation with a 2.5 kW PV string. Its operating voltage varies in 350 ± 50 V range during PV cell temperature variations when interfaced into 350 V dc bus.

It was also proven that the proposed converter can smoothly change the polarity of the series port, enabling smooth transitions between its operating quadrants when using a linear controller. This feature is unique among the known step-up/down PPCs, preventing possible MPPT efficiency drops. This feature, combined with simplicity, high efficiency, and low cost, makes the proposed PPC a superior solution for PV string applications in dc microgrids.

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