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Magnetically Integrated Multiport Converter for Energy Management in DC-Powered Buildings

Edivan Laercio Carvalho[1], Andrii Chub[1], Andrei Blinov[1], Satish Naik Banavath[2], Dmitri Vinnikov[1]

[1]Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology, Tallinn, Estonia
[2]Department of Electrical, Electronics, and Communication Engineering, Indian Institute of Technology Dharwad, India

e-mail: edivan.carvalho@taltech.ee, andrii.chub@taltech.ee, andrei.blinov@taltech.ee, satish@iitdh.ac.in, dmitri.vinnikov@taltech.ee

ABSTRACT Multiport converters have gained attention in the last few years as a key component for dc-powered buildings, more electric aircraft, and maritime applications. For buildings, the prevalence of dc appliances and electronic loads increases the need for efficient integration with both ac grid and local generation. Ac-dc multiport converters play an important role in this integration because dc distribution has been considered for power integration in modern buildings. In addition, the growing complexity of loads and sources within buildings has driven interest in developing flexible solutions to provide highly efficient integration. Furthermore, ongoing developments in standardization for in-building dc grids underscore the importance of considering specific requirements for future designs. This paper proposes a multiport power converter (ac/dc/dc) to integrate dc-powered buildings into an ac grid. By providing a multiport solution, it is possible to reduce the power processing stages and the component count. To evaluate the effectiveness of this concept, a 5-kW prototype was built and tested, including efficiency evaluation. In addition, emerging standards are discussed to tailor the power converter design for building applications.

KEYWORDS Bidirectional power flow, dc-powered buildings, energy efficient buildings, multiport converters, isolated converters.

I. INTRODUCTION

The buildings' energy efficiency holds significant global importance for the energy transition. Notably, the European Union (EU) targets enhancing energy efficiency of buildings as they account for 40% of energy consumption [1]–[2]. This concern is even more critical in northern countries like Estonia, where energy consumption in buildings surpasses the EU average, comprising 50% of the total energy usage. Key contributors to this high energy consumption include electronic devices, lighting, and heating systems, with the latter being particularly critical [1]. Approximately 80 % of energy consumed in EU households is allocated to space heating and water heating, as presented in Fig. 1 [2].

In response to these pressing concerns, the EU has initiated a series of initiatives and directives aimed at enhancing the energy efficiency of buildings. These actions are designed to incentivize or compel consumers to save energy and improve their electrical installations [2]. The main directive pertinent to this context is the Energy Performance of Buildings Directive (EPBD) [1]. The EPBD encompasses a range of provisions for buildings, including recommendations for enhancing energy efficiency, strategies for renovations, and labeling of energy performance. Regarding the labeling, to achieve a very high efficiency level, denoted as "A-class," it is necessary for buildings to limit energy consumption significantly throughout the year. These buildings are referred to as nearly zero-energy buildings (NZEB) and typically employ highly efficient devices, on-site renewable generation, and, possibly, energy

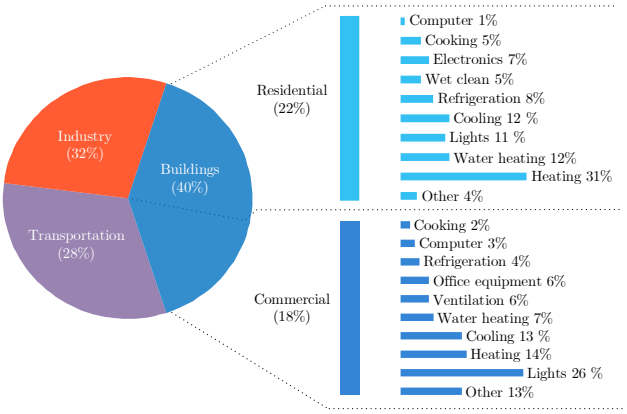


FIGURE 1. Share of energy consumption by sectors [2].

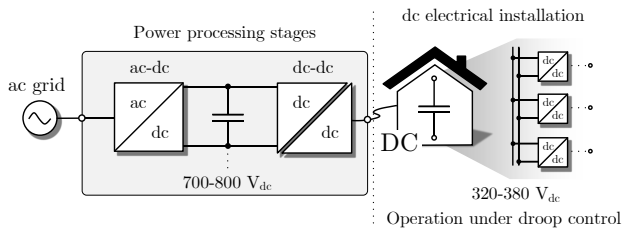


FIGURE 2. Schematic overview for ac grid and dc-powered buildings integration.

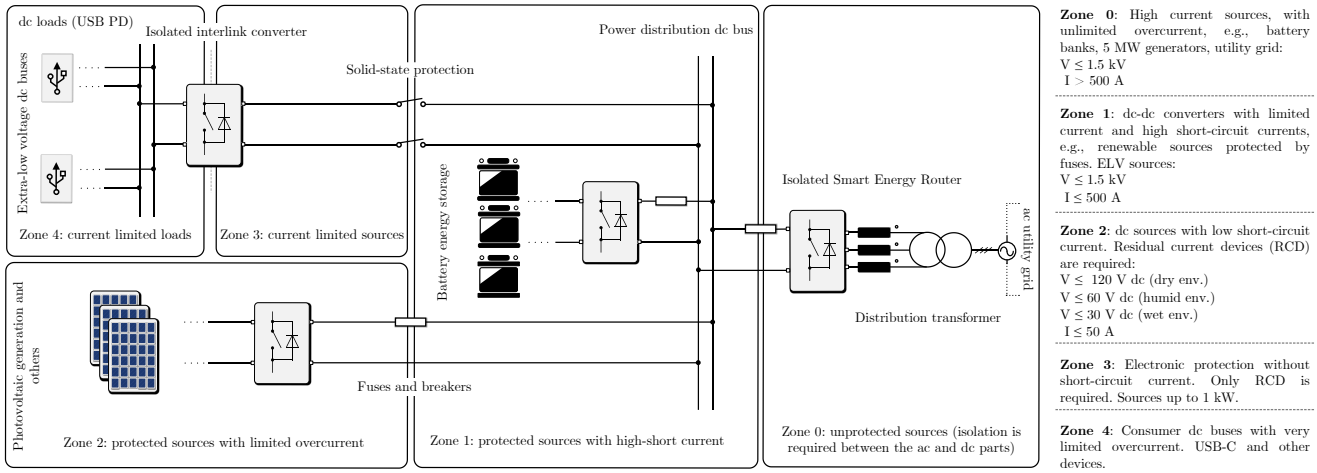


FIGURE 3. Isolation requirements and safety zones in the dc distribution system according to NPR 9090, and [3].

storage [3]. Moreover, the EU revised the EPBD in May 2024 to introduce the concept of zero-emission buildings, which must not emit any carbon from fossil fuels, in addition to high energy efficiency. The new requirements will become compulsory from 2023 for newly commissioned buildings.

One significant challenge related to buildings is energy waste related to power electronic devices that have several power processing stages to connect to ac grid [3]–[4]. For example, rectifiers are responsible for reducing efficiency and power factor, since power factor correction is typically not required for low-power applications [5]. However, considering a commercial building with multiple floors, for example, or even residential ones, the cumulative energy waste becomes significant, even for installations where low-power devices are dominant.

One of the emerging and promising solutions to save energy is to use dc distribution inside buildings. The dc buildings use dc power distribution to integrate on-site generation and energy storage [3]. In this case, it is possible to simplify the power electronics interfaces and mitigate problems related to multiple energy conversion stages since, currently, dc loads are adapted to ac using a rectifier stage.

Fig. 2 presents a sketch of a dc building where an ac-dc converter is used to provide integration between ac grid and dc microgrid inside the building. This concept has become more and more popular in the last few years. However, problems related to standardization are still a challenge to overcome because protection requirements are quite critical for dc. Nowadays, there are several initiatives aimed at standardizing dc electrical installations, including the IEC 60364-series in development [6], Dutch NPR9090 [7], and Current/OS Foundation's protocol [8]. NPR9090 was the very first set of practical guidelines for dc systems, implemented in the Netherlands in 2018 [9], and there is currently an updated version from 2024 [8]. This standard provides interesting information for current designs and upcoming international standards, including protection zones, isolation requirements, voltage levels, grounding schemes, etc. Fig. 3 presents the main voltage levels, isolation requirements, and protection zones for dc electrical installations, according to NPR9090.

Galvanic isolation from ac grid is an important requirement for dc buildings due to leakage current, grounding, and safety requirements, especially considering that most loads come into direct contact with end users. Following current standards, it is mandatory to provide isolation between ac grid and dc distribution inside buildings [6]–[8]. Because of this reason, isolated ac-dc converters are used for the ac grid integration. In the Current/OS protocol, such converters are called as active front-end converters (AFE), and they are responsible for the power sources and loads integration inside buildings, including ac grid [8].

A common solution to provide isolation for AFE converters is to use two-stage power converters, where an ac-dc stage is used for the ac grid connection, while an additional dc-dc stage provides isolation for a dc building [10]. For the residential level, three-phase 230 V_{rms} are used at the ac side, while 350 V_{dc} is defined by Current/OS for power distribution inside buildings [8]. On the other hand, most consumer electronic loads and lighting operate at extra-low voltage dc (ELVDC). ELVDC increases safety because electric shocks are not risky at this voltage level (36-57 V_{dc}), making it suitable for low-power loads [4]. However, according to Fig. 3, isolation is also needed between ELVDC (24-60 V_{dc}) and power distribution bus (350 V_{dc}), as an isolated interlink converter is necessary. In addition, Fig. 3 presents the protection requirements, voltage and current levels, according to the defined zones, as specified by the NPR9090 standard [7], and interpreted in [3].

A variety of power electronics solutions can be used to meet such requirements, including multistage and multiport converters. The simplest way to provide isolation for ELVDC is to use an additional isolated dc-dc converter. Although such solutions, connected to 700 V_{dc} or 350 V_{dc} buses, can be based on well-known technologies such as phase-shift full-bridge [11]–[12] or series-resonant converters [13]–[15], this additional dc-dc stage would contribute to the reduction of the overall system efficiency, and to increase the component counting.

A possible solution to avoid redundant power processing stages is to achieve the integration of different buses by using a multiport converter. In this case, a multi-winding transformer is utilized in a single dc-dc converter to provide isolation for an additional ELVDC port [16]–[17], reducing the number of components and power stages. Multiport converters have been employed in many applications before, including solid-state transformers [17]–[19], hybrid energy storage systems [20], and bipolar dc microgrids [21]. Many of these applications have clearly defined requirements, demanding bidirectional power flow, which justifies the usage of three active bridges. However, such converter

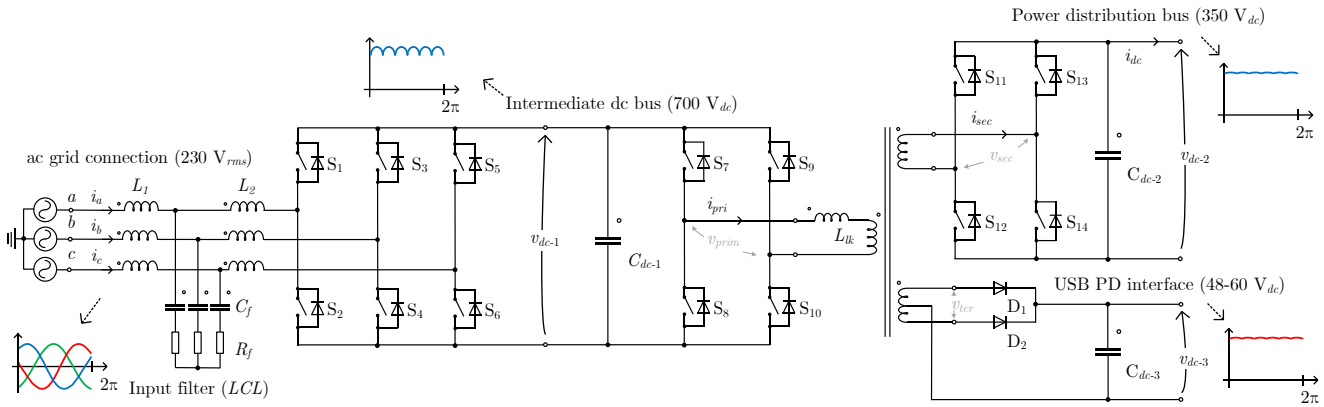


FIGURE 4. Proposed multiport converter based on a two-level voltage source converter (ac-dc), dual-active bridge (dc-dc), and center-tapped rectifier (USB PD interface).

usually has problems related to circulating current and complexity.

In addition, the emergence of new standards for dc buildings enables the development of new solutions tailored to meet application requirements. In this paper, a multiport solution is proposed to comply with the Current/OS protocol, which does not require bidirectional operation of the ELVDC port. The presented topology is based on two stages: a non-isolated ac-dc stage for ac grid integration and power factor correction and a three-port isolated dc-dc converter, as presented in Fig. 4. The dc-dc stage is designed to provide a 350 V_{dc} bus for the power distribution inside a building, while an ELVDC port (36-57 V_{dc}) allows direct connection with loads. This concept was introduced for the first time in [16], while the presented paper is an extended version, including analysis of standards, power converter's design guidelines, experimental results, and detailed comparison.

To evaluate this concept, a 5-kW prototype was built, and laboratory tested. The experimental results evaluate the converter efficiency, waveforms, and main functionalities to meet the dc buildings' requirements. In the following, the paper is organized into five different sections: Section II presents the application requirements according to the current standards and directives; Section III presents the power converter description; Section IV presents the experimental results; and finally, Section VI presents the main conclusions.

II. APPLICATION REQUIREMENTS

The main directives to standardize dc systems are found in the IEC6034 series, NPR9090, and Current/OS [6]–[8]. These standards cover several aspects of dc electrical installations and can be used as directives for dc buildings. In addition, reference [3] presents an overview related to standards, functionalities, and power converter topologies for grid integration of buildings. The main requirements for dc buildings are discussed below.

A. *COMPATIBILITY WITH AC GRID AND POWER QUALITY*

The grid integration of dc buildings is defined by standards related to power quality, power factor correction, voltage fluctuation, and others. The main standards to be cited are the IEC 61000-3 [6], IEC TC 62786-1:2023 [22] and [23], related to distributed energy resources connection with the grid.

In terms of design requirements, the most important ones for the AFE converters are related to total harmonic distortion (THD), power factor control (PFC), and individual harmonics emission.

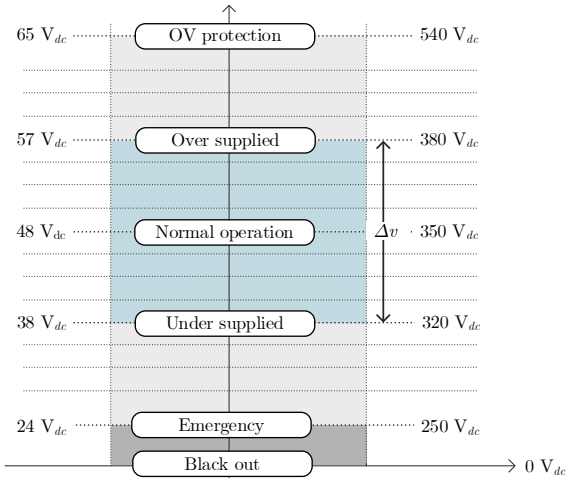


FIGURE 5. Current/OS voltage ranges for 48 V, and 350 V dc systems.

Ideally, the THD should be lower than 5% at nominal power, with a power factor of >0.98 for the whole operating range.

B. *DROOP CONTROL AND DC GRID COMPATIBILITY*

Droop control requirements are discussed in the Current/OS system reference document to ensure compatibility between dc grid, loads, and other power electronics devices [8]. The current directives NPR9090 and Current/OS define the allowed voltage fluctuation as presented in Fig. 5. This defines the voltage deviation (Δv) used to calculate the droop coefficient (m). The droop coefficient is given by (1)

$$m = \frac{\Delta v}{i_{max}} \tag{1}$$

where i_{max} is the maximum processed current, for a given power converter.

C. *VOLTAGE LEVELS AND NORMAL OPERATION*

The voltage bands defined by Current/OS protocol are presented in Fig. 5. Additionally, [8] also defines the converter operation under overvoltage (OV), and undervoltage, time of disconnection, and protection devices requirements for abnormal operating conditions.

D. *ELVDC REQUIREMENTS*

According to Fig. 5, ELVDC levels are also defined by standards to supply light loads and appliances, which usually can be in direct contact with the end-users. ELVDC increases

safety because electric shocks are not a risk at this voltage level. However, the isolation is a mandatory requirement for fault isolation due to the leakage current issues.

Following the NPR9090 and Current/OS protocol, the main isolation requirements are presented in Fig. 3. The isolation between ac and dc parts is necessary to isolate faults between both systems. This is an important requirement since it allows for simplifying the grounding schemes and protection.

For example, considering a unipolar system, a TN-S grounding is possible using only one overcurrent protection device (OCPD). For the ELVDC, the main issues are related to the leakage current and end-user safety. Ensuring isolation makes direct contact with dc buses possible without risks for the end-users. Additionally, NPR9090 defines protection zones according to the available fault energy, isolation, and voltage levels, which can be used as design guidelines [8].

E. *USB PD AS A NEW STANDARD*

Many devices charge or get power from USB plugs, including laptops, phone chargers, TV sets, and other appliances. In addition, in the last few years, USB technologies, like new standards for USB power delivery (USB PD) 3.1, continuously increased maximum power level. As an open, widely adopted standard, this technology is being adopted by increasingly more electronic devices. Fig. 6 presents an overview of power requirements for extra-low voltage loads, which currently use USB PD as the main standard. Additionally, Fig. 6 presents the power delivered by different USB PD standards. As USB PD is the most popular standard for many electronic devices, modern buildings are expected to have USB PD as the main wall sockets. Because of this reason, USB PD levels are already included in the Current/OS protocol and NPR9090 and should be provided by the proposed multiport converter.

III. POWER CONVERTER DESCRIPTION

Based on the isolation requirements, voltage levels, power, and functionalities discussed in Section II, the multiport converter presented in Fig. 4 is proposed as a solution for building integration. For the ac-dc stage, 700 V_{dc} was defined as an intermediate dc bus voltage ($v_{dc\text{-}1}$). This value is common for LVDC applications, and it is enough to synthesize a sinusoidal voltage of 230 V_{rms} at the ac side.

For the dc power distribution ($v_{dc\text{-}2}$), and ELVDC output ports, voltage levels of 350 V_{dc} and 48-60 V_{dc}, respectively, were selected to follow the standard requirements.

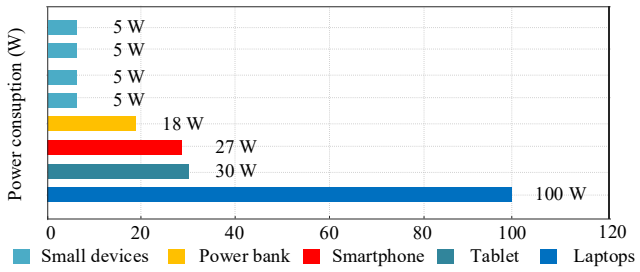


FIGURE 6. Overview of the typical power levels of different types of devices based on USB PD.

A. *POWER FACTOR CORRECTION STAGE*

Several implementation possibilities exist for the ac-dc stage, including multi-level and totem pole PFC. The totem pole PFC is very popular for power factor correction due to the possibility of working as an interleaved converter [24].

However, it increases the number of semiconductors and passive elements. For example, considering a simple, totem-pole PFC without any additional interleaved cells, the number of active semiconductors is equal to 12 for a three-phase solution, while a simple two-level voltage source converter (2L-VSC) can provide a similar solution with only 6.

Being very well-known, and widely adopted in industry, the 2L-VSC topology was adopted for the PFC stage. For the filter design, a third-order (LCL) filter is preferable due to the higher attenuation factor when compared to the first-order ones (L) [25]. Considering the LCL filter presented in Fig. 4, the three-phase system can be decoupled into three single-phase ones, defined by the transfer function (2), where U_{pwm} is the converter voltage, and i_{L1} is the output current related to the phase currents (i_a, i_b, i_c).

$$\frac{i_{L1}(s)}{U_{pwm}(s)} = \frac{s \cdot C_f \cdot R_f + 1}{s^3 \cdot C_f \cdot L_1 \cdot L_2 + s^2 \cdot C_f \cdot (L_1 + L_2) + s \cdot (L_1 + L_2)} \tag{2}$$

From (2), it is possible to define the main parameters to design the LCL filter, including natural frequency (ω_n), damping factor (ξ), and resonance frequency (ω_{res}), given by 3, 4, and 5, respectively.

$$\omega_n = \sqrt{\frac{L_1 + L_2}{C_f \cdot L_1 \cdot L_2}} \tag{3}$$

$$\xi = \frac{R_f \cdot (L_1 + L_2)}{2 \cdot \omega_n \cdot L_1 \cdot L_2} \tag{4}$$

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{C_f \cdot L_1 \cdot L_2} - \frac{1}{2} \cdot \frac{R_f \cdot (L_1 + L_2)}{L_1 \cdot L_2}} \tag{5}$$

In addition, the filter attenuation (K_s) for a given switching frequency (ω_s) is by (6),

$$K_s = \left| \frac{C_f \cdot R_f \cdot \omega_s + 1}{D} \right| \tag{6}$$

where, $D = -j\omega_s^3 L_1 L_2 C_f - \omega_s^2 \, C_f \, R_f \, (L_1 + L_2) + j\omega_s (L_1 + L_2)$. K_s is related to the total harmonic distortion (THD) according to (7).

$$K_s \leq \frac{\sqrt{2} \cdot i_{L2} \cdot \mathrm{TDH}}{U_{pwm}} \tag{7}$$

TABLE I
LCL filter design parameters

Parameter	Value
Intermediate dc bus voltage ($v_{dc\text{-}1}$)	700 V
Resonance freq. (ω_{res})	$2 \cdot \pi \cdot 25$ kHz
Switching frequency (f_s)	100 kHz
Damping factor (ξ)	0.707
Attenuation factor (K_s)	0.04
Total harmonic distortion (THD)	5%
L_1	20 µH
L_2	20 µH
C_f	4.7 µF
R_f	0.5 Ω

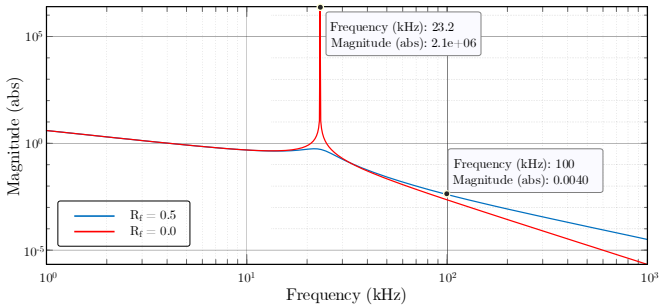


FIGURE 7. Frequency response for the undamped and a damped designed filter.

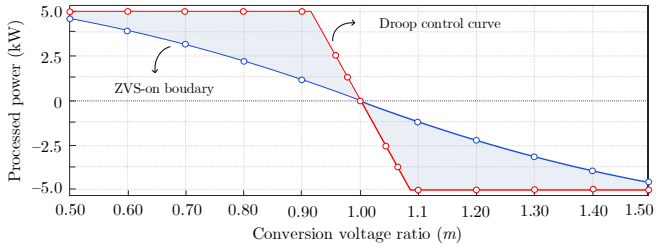


FIGURE 8. Comparison between DAB converter's soft-switching regions and effective operation areas, limited according to the droop curve.

Following the methodology presented in [26], it is possible to solve the set of equations, (3)–(7) to determine L_1, L_2, C_f, and R_f. Considering the parameters presented in Table I, the values of LCL filter elements are defined as $L_1 = 20$ µH, $L_2 = 20$ µH, $C_f = 4.7$ µF, and $R_f = 0.5$ Ω. To verify the design of the filter, Fig. 7 presents the resulting frequency response where the resonant frequency of 23.4 kHz is evident, and the attenuation factor is equal to 0.04 at the switching frequency (100 kHz).

B. *ISOLATION STAGE*

A dual-active bridge (DAB) converter is used to provide the galvanic isolation between the PFC output ($v_{dc\text{-}1}$), and dc distribution bus ($v_{dc\text{-}2}$). Essentially, this converter should have bidirectional power transfer capability due to the possible on-site energy generation and storage. In addition, the main isolation stage is designed to supply the total building capacity, while the additional ELVDC port is naturally limited to a range of relatively low-power loads. Because of this reason, both isolation stages are designed as two decoupled converters.

To design the DAB converter, the methodology presented in [10] is followed, considering that the power transfer is given by (8).

$$P = \frac{(n_1{:}n_2)\cdot v_{dc\text{-}1}\cdot v_{dc\text{-}2}\cdot \delta\cdot(\pi-\delta)}{2\,\pi^{2}\cdot f_s\cdot L_{lk}} \tag{8}$$

The transformer turns ratio $(n_1{:}n_2)$ is directly defined by the nominal voltage levels $v_{dc1} = 700$ V, and $v_{dc2} = 350$ V, following the previously defined parameters. Ideally, $n_1{:}n_2$ is selected to result in a unitary voltage gain to reduce the maximum phase-shift ratio (δ) as much as possible. As a design criterion, it is assumed that the maximum phase-shift ratio is equal to 30 deg [10]. Therefore, from (8), it is possible to define the leakage inductance (L_{lk}).

For the DAB stage, the ZVS-on is defined according to (9), where C_{oss} is the equivalent total output capacitance intrinsic for the semiconductors.

$$\frac{1}{2}\,L_{lk}\,(i_{zvs})^2 \geq \frac{1}{2}\,C_{oss}\,(v_{dc\text{-}1})^2 \tag{9}$$

To ensure (9), the following conditions must be satisfied:

$$\begin{cases} i_{zvs} > 0 \text{ being, } \delta > \frac{\pi}{2}\cdot\left(1-\frac{1}{m}\right) \\ i_{zvs} > 0 \text{ being, } \delta > \frac{\pi}{2}\cdot(1-m) \end{cases} \tag{10}$$

Substituting (10) in (8), it is possible to define the boundaries between soft- (ZVS-on) and hard-switching, as given by (11) and (12).

$$P(m)\big|_{i_{zvs}} = \frac{v_{in}^{2}\cdot\frac{\pi}{2}\cdot\left(1-\frac{1}{m}\right)\cdot\left(\pi-\frac{\pi}{2}\cdot\left(1-\frac{1}{m}\right)\right)}{m\cdot 2\pi^{2}\cdot 2\,\pi^{2}\cdot f_s\cdot L_{lk}} \tag{11}$$

$$P(m)\big|_{i_{zvs}} = \frac{v_{in}^{2}\cdot\frac{\pi}{2}\cdot(1-m)\cdot\left(\pi-\frac{\pi}{2}\cdot(1-m)\right)}{m\cdot 2\pi^{2}\cdot 2\,\pi^{2}\cdot f_s\cdot L_{lk}} \tag{12}$$

Considering a leakage inductance $L_{lk} = 60$ µH defined according to the methodology presented in [10], Fig. 8 compares the soft-switching boundaries and the droop control curve, defined according to the Current/OS protocol. According to the presented results, it is possible to notice that, when operating under droop control, the converter's effective operation area is narrowed down to a line, enabling the power converter to operate within its full soft-switching range. This is a very beneficial feature of adopting a DAB converter in this specific application. In addition, [10] presents all soft-switching conditions for DAB converter operating under droop control and should be used as a complementary reference for the DAB converter design.

C. *ELVDC PORT*

Finally, the ELVDC port ($v_{dc\text{-}3}$) is implemented by adding a winding to the isolation transformer. Ideally, it is necessary to decouple $v_{dc\text{-}2}$ and $v_{dc\text{-}3}$, since $v_{dc\text{-}2}$ is a variable voltage due to the droop control operation. In practice, stabilizing $v_{dc\text{-}3}$ is unnecessary. However, it is necessary to ensure a certain voltage level compatible with USB PD standards, e.g., between 48 V_{dc} and 60 V_{dc}. Therefore, when considering magnetically integrated solutions, it is necessary to minimize cross-coupling between $v_{dc\text{-}3}$ and $v_{dc\text{-}2}$, where droop control is applied. In other words, it is important to decouple $v_{sec.}$ and $v_{ter.}$ windings to ensure a proper voltage level for $v_{dc\text{-}3}$.

To establish a dc stable link on the ELVDC side, ideally, the tertiary winding is positioned as close as possible to the primary side, where 700 V_{dc} is defined as a fixed input voltage. The mutual inductances L_{13}, and L_{23}, are given by (13) and (14), being k' and k'' the coupling factor between windings 1-3, and 2-3, respectively, and L_1, L_2, and L_3, being the self-inductances.

$$L_{13} = k'\cdot\sqrt{L_1\cdot L_3} \tag{13}$$

$$L_{23} = k''\cdot\sqrt{L_2\cdot L_3} \tag{14}$$

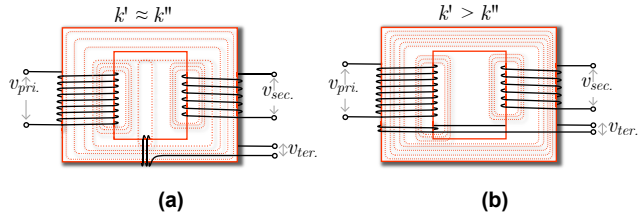


FIGURE 9. Examples of transformer designs: (a) moderate coupling factor (*k*") between secondary and tertiary windings and (b) low coupling factor (*k*") between secondary and tertiary windings.

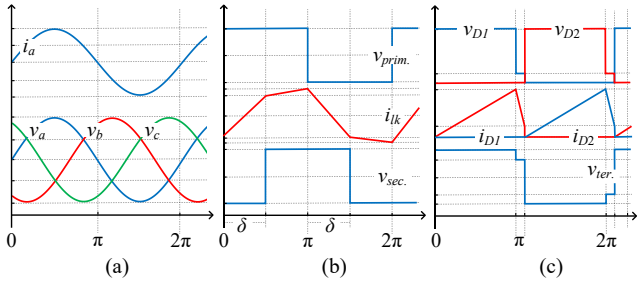


FIGURE 10. Main waveforms for the proposed converter: (a) sinusoidal waveforms from the ac-dc converter; (b) dual-active bridge converter waveforms, operating with phase-shift modulation; and (c) rectifier for the USB PD interface.

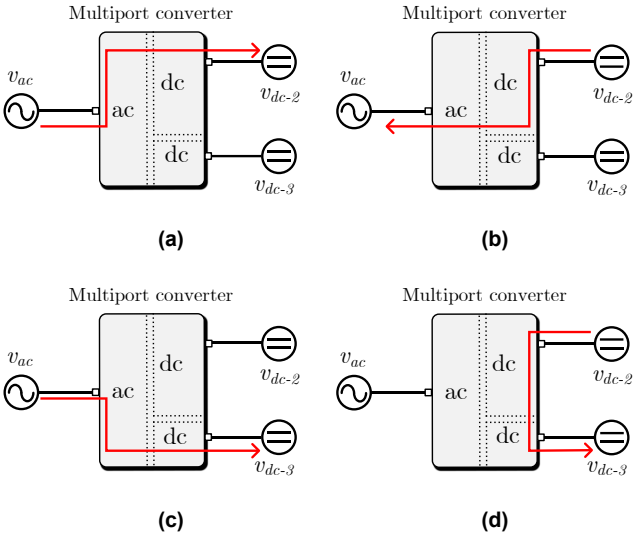


FIGURE 11. Multiport converter's operation modes: (a) Mode I – power flow from v_{ac} to $v_{dc\text{-}2}$; (b) Mode II – power flow from $v_{dc\text{-}2}$ to v_{ac}; (c) Mode III – ELVDC is supplied by v_{ac}; (d) Mode IV – ELVDC is supplied by $v_{dc\text{-}2}$.

Fig. 9 presents two examples of transformer design and how to reduce coupling between secondary and tertiary windings. Since mutual inductances depend on k' and k'', as shown in (13) and (14), it is observed from Fig. 9 that by adjusting the winding position, it is possible to reduce the coupling factor between the second and third windings to avoid undesirable voltage variations at the tertiary side. Fig. 10 presents the main waveforms for each power processing stage, including the sinusoidal waveforms for the ac-dc converter; the DAB is operating with phase-shift modulation, and the passive rectifier at the ELVDC side.

D. *OPERATION MODES*

The proposed multiport converter presents four basic operation modes, which are defined according to the power flow. Additional sub-modes are also possible, those being a combination of the main ones.

Mode I, Fig. 11a: positive power flow, coming from ac grid (v_{ac}) to the main dc power distribution bus $(v_{dc\text{-}2})$.

Mode II, Fig. 11b: negative power flowing from the dc grid $(v_{dc\text{-}2})$ to ac utility grid (v_{ac}).

Mode III, Fig. 11c: when the ELVDC bus $(v_{dc\text{-}3})$ is supplied from the ac grid (v_{ac}).

Mode IV, Fig. 11d: when the ELVDC bus $(v_{dc\text{-}3})$ is supplied from the dc grid $(v_{dc\text{-}2})$.

IV. EXPERIMENTAL RESULTS

According to the design parameters presented in Tables I and II, a prototype was built, and laboratory tested. The experimental setup is presented in Fig. 12, including the ac-dc converter, dual-active bridge, high-frequency transformer, filters, dc buses, and the additional extra-low voltage port. The main converter's waveforms were obtained with an oscilloscope Tektronix DPO4034, while the efficiency curves and power quality were measured with the power analyzer Yokogawa WT1800E. Related to the converters modeling and control system, [27] and [28] can be used as complementary references for the dc-dc stage, while [29]-[31] present the control and modeling for the ac-dc.

A. *PRIMARY PORT - AC-DC STAGE*

Experimental results are presented for each power processing stage to demonstrate the power converter operation. Fig 11 presents the main waveforms for the ac-dc stage, which is responsible for the ac grid integration.

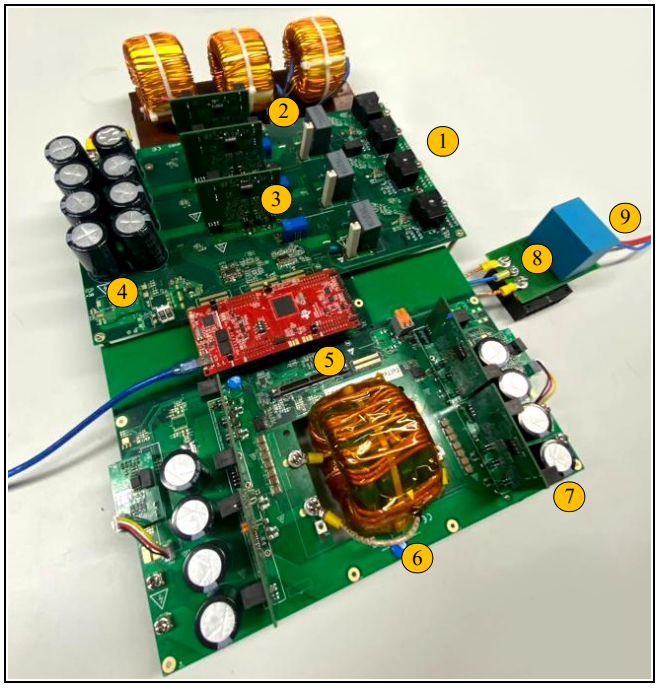


FIGURE 12. Experimental prototype, including: (1) ac grid connection; (2) *LCL* filter; (3) ac-dc converter; (4) intermediate dc bus (700 V_{dc}); (5) dual-active bridge converter; (6) multi-winding transformer; (7) distribution dc bus (350 V_{dc}); (8) center-tapped rectifier at extra-low voltage; (9) USB PD output.

TABLE II
Main specifications and parameters for the dc-dc stages

Parameter/Component	Value/Detail
Nominal power (P_o)	5.3 kW
Input dc bus voltage ($v_{dc\text{-}1}$)	700 V_{dc}
Power distribution dc voltage ($v_{dc\text{-}2}$)	320-380 V_{dc}
Extra-low voltage dc bus ($v_{dc\text{-}3}$)	48-60 V_{dc}
Switching frequency (f_s)	100 kHz
Phase-shift range (δ)	$-\pi/6 \leq \delta \leq \pi/6$
HF transformer	Pri: 24 turns Sec: 12 turns Ter: 4 (2:2) turns. Core: 4×B64290L0730 (N87) Total leakage inductance: 60 µH
Capacitor $C_{dc\text{-}1}$	220 µF
Capacitor $C_{dc\text{-}2}$	470 µF
Capacitor $C_{dc\text{-}3}$	60 µF
Primary side switches	C2M0160120D (1200 V/19 A) 160 mΩ /47 pF
Secondary side switches	C3M0120065D (650 V/22 A) 120 mΩ /45 pF
Tertiary side diodes	VB20150SG (150 V/20 A)
Driver circuit	UCC21521

Processing 5 kW, the resulted *rms* current is 7.3 A_{rms}, while 230 V_{rms} were measured for each phase (v_a, v_b, and v_c), as shown in Fig. 13 (a). These results present maximum THD at 0.5 kW, equal to 4.86%, per the *LCL* filter design and requirements presented in Section II (a).

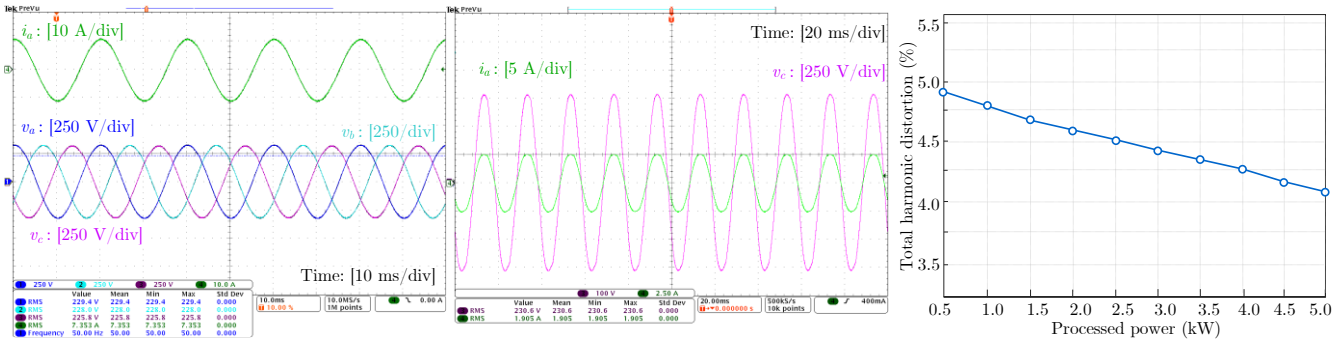
B. *SECONDARY PORT - DAB STAGE*

Fig. 14 presents the main waveforms for the dual-active bridge converter. The experimental results include the transformer voltages (v_{prim}, v_{sec}), leakage current in the secondary side (i_{sec}), and output voltage ($v_{dc\text{-}2}$). The presented tests were performed to verify the voltage regulation in the secondary side, which should follow the droop control line from Fig. 8. Fig. 14 (a) presents the result when 2 kW is processed with positive power flow from $v_{dc\text{-}1}$ to $v_{dc\text{-}2}$. The output voltage is equal to 336 V. While the processed power is increased, the output voltage should decrease to follow the droop control line.

Fig. 14 (b) presents the experimental results when the processed power is equal to 5 kW. The measured output voltage is 320 V, since this is the voltage limit according to the Current/OS requirements presented in Fig. 5. For the negative power flow, the voltage limit is equal to 380 V, and the transformer current is in the opposite phase with the transformer voltages, as presented in Fig. 14 (c). Following the presented results, it is possible to verify that the DAB stage can follow the droop control line, presented in Fig. 8. This is a very important feature for the proposed power converter, since the operation under droop control is a mandatory requirement according to the Curren/OS protocol.

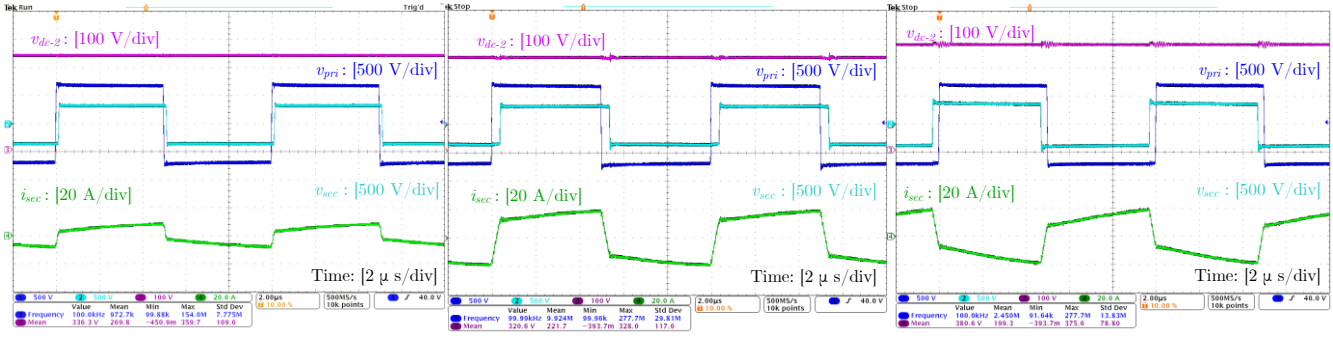
C. *EXTRA-OW VOLTAGE PORT*

Fig. 15 presents the main waveforms for the passive rectifier at the ELVDC side. Under the same conditions as presented in the experimental test of Fig. 15 (a), the waveforms for the tertiary side were obtained, including the transformer voltage ($v_{ter.}$), diode voltages (v_{D1}, v_{D2}), and current (i_{D1}). Both



(a) (b) (c)

FIGURE 13. Experimental results for the ac-dc stage, including: (a) phase a current (i_a), and phase voltages (v_a, v_b, and v_c); (b) power factor verification (v_a, i_a); and (c) current THD for different power levels.



(a) (b) (c)

FIGURE 14. Experimental results for the DAB stage, including: (a) transformer voltages (v_{pri}, and v_{sec}), transformer current (i_{sec}), and output voltage ($v_{dc\text{-}2}$) for 2 kW of processed power; (b) 5 kW of processed power; and (c) –5 kW of processed power.

diode voltages are complementary, and their current is triangular, as predicted theoretically in Fig. 10.

To test the rectifier stage at different power levels, Fig. 15 (b) and Fig. 15 (c) present the experimental results for 140 W and 200 W of processed power. In both cases, the output voltage is approximately 52 V, which is in accordance with the specifications for the USB PD interface. This means that, even with load variations, there are no significant changes in the output voltage since the transformer tertiary side is strongly coupled only with the primary side winding ($v_{dc\text{-}1}$) with a fixed input voltage of 700 V.

Fig. 16 presents the experimental waveforms of the transformer voltages, $v_{prim.}$, $v_{sec.}$, and $v_{ter.}$. According to the transformer turns ratio (n_1: n_2: n_3), the primary voltage is reduced to produce different voltage levels at the outputs $v_{dc\text{-}2}$ and $v_{dc\text{-}3}$. In addition, it is possible to observe a phase shift between $v_{prim.}$ and $v_{sec.}$, resulting from the DAB converter modulation. This follows the theoretical waveforms presented in Fig. 10. The resulted output voltage ($v_{dc\text{-}3}$) at the ELVDC port is equal to 51.81 V, while 336 V is achieved in the secondary side ($v_{dc\text{-}2}$).

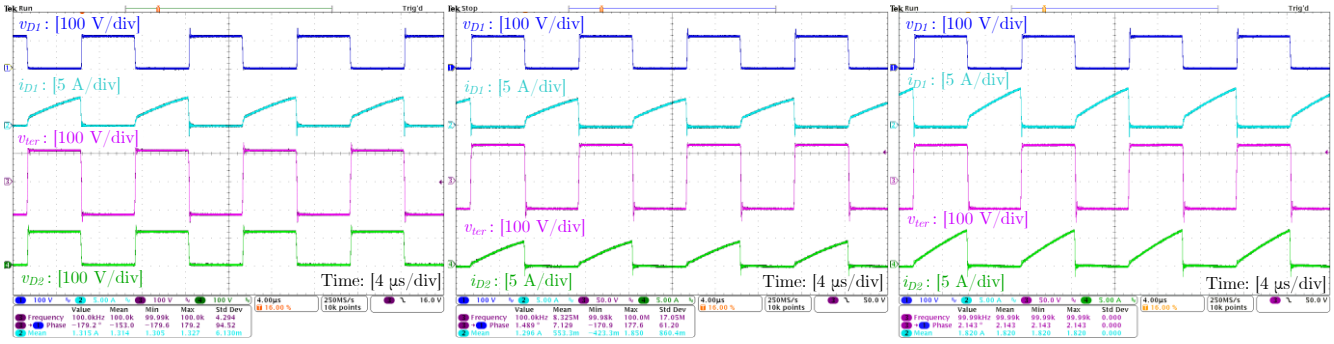
To verify the voltage deviation in the ELVDC side, Fig. 16 (b) and Fig. 16 (c) present the experimental results, considering different output voltages on the secondary side ($v_{dc\text{-}2}$). Given that the dc distribution bus ($v_{dc\text{-}2}$) experiences voltage variations due to droop control requirements, it is necessary to verify how these variations can affect the ELVDC port ($v_{dc\text{-}3}$). Fig. 16 (b) presents the experimental results considering $v_{dc\text{-}2}$ equal to 320 V. The resulting output voltage at the ELVDC side $v_{dc\text{-}3}$ is equal to 52.58 V_{dc}. Fig. 16 (c) presents the experimental results when $v_{dc\text{-}2}$ is equal to 380 V. In this case, the output voltage at the ELVDC port is equal to 52.48 V. Both results follow the design requirements presented in Fig. 5.

D. *EFFICIENCY EVALUATION AND COMPARISONS*

To provide additional insight about the converter design, experimental results were taken to compare two different transformer designs, being k' the coupling factor between primary and tertiary windings, and k'' the coupling factor between secondary and tertiary windings. Fig. 17 (a) presents the voltage regulation in $v_{dc\text{-}2}$ and $v_{dc\text{-}3}$, considering a fixed input voltage (700 V), and droop control operation at the secondary side. For this first case, it is considered that $k'>k''$, since the transformer design has been made to ensure decoupling between the secondary and tertiary windings. According to the experimental results, it is possible to observe that there are no significant voltage variations at the ELVDC port ($v_{dc\text{-}3}$) for this case. However, when $k'\approx k''$, the voltage variation increases in the ELVDC side, due to the cross-coupling issues.

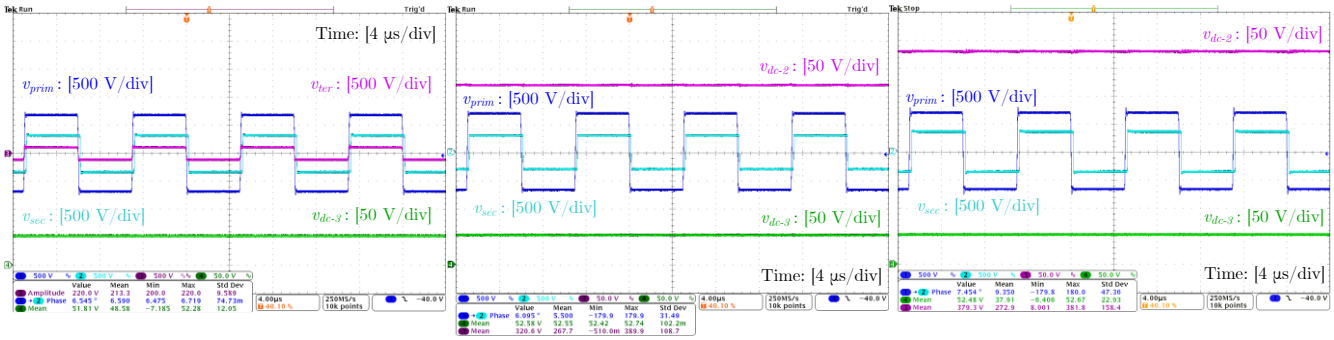
Fig. 17 (b) compares both cases, considering $k'\approx k''$, and $k'>k''$. Therefore, to meet the Current/OS protocol's requirements, it is necessary to design the isolation transformer to reduce coupling between the secondary and tertiary windings as much as possible.

To evaluate the converter efficiency, the power analyzer Yokogawa WT1800 was used to measure the multiport converter efficiency in different operation modes. Fig. 18 (a) presents the experimental results of operation mode I, where the power is processed between v_{ac} and $v_{dc\text{-}2}$.



(a) (b) (c)

FIGURE 15. Experimental results for the ELVDC port: (a) main waveforms, including v_{ter}, v_{D1}., i_{D1}., and v_{D2}; and tests for different power levels, including (b) 140 W; and (c) 200 W of processed power.



(a) (b) (c)

FIGURE 16. Experimental results for the voltage deviation in the ELVDC port: (a) transformer ($v_{prim.}$, $v_{sec.}$, and $v_{ter.}$) and output voltages ($v_{dc\text{-}3}$); and considering different output voltages at the secondary side being: (b) $v_{dc\text{-}2}$ = 320 V; and (c) $v_{dc\text{-}2}$ = 380 V.

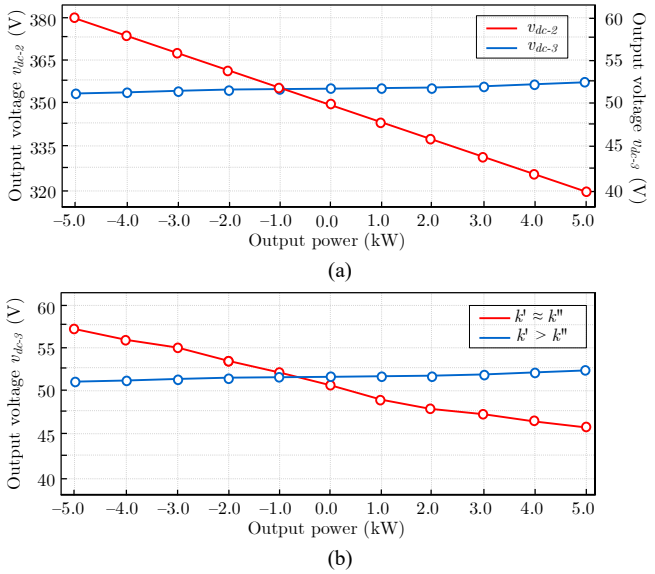


FIGURE 17. Experimental results for the voltage variation in the ELVDC side: (a) resulted voltage variation in the tertiary side (v_{dc-3}), considering droop control at the secondary, being ($k'>k''$).; and (b) comparison between voltage variations in the tertiary side, considering two different transformer designs ($k'\approx k''$ and $k'>k''$). (to mention the power 300 W)

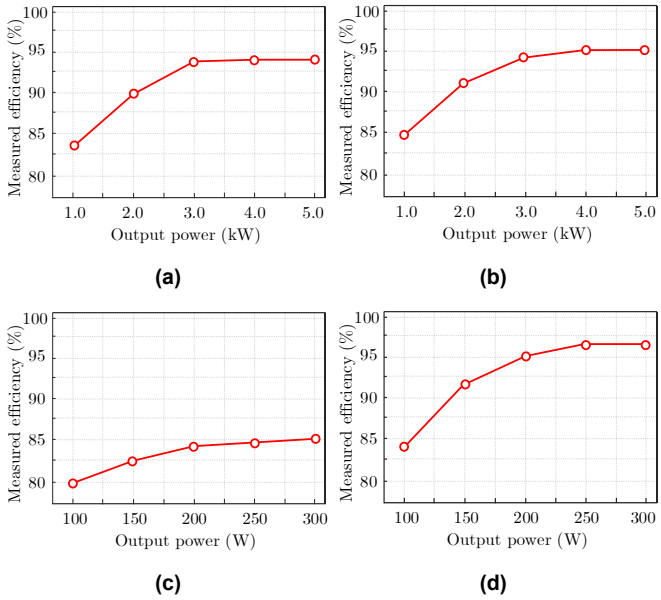


FIGURE 18. Experimental efficiency curves for different operation modes: (a) Mode I – power flow from v_{ac} to v_{dc-2}; (b) Mode II – power flow from v_{dc-2} to v_{ac}; (c) Mode III – power flow from v_{ac} to v_{dc-3}; (d) Mode IV – power flow from v_{dc-2} to v_{dc-3}.

In this case, the multiport converter processes up to 5 kW of output power, and the output voltage v_{dc-2} varies between 350 V and 320 V, according to the droop control curve presented in Fig. 8, and Current/OS requirements. The resulting peak efficiency is equal to 94.6%.

Fig. 18 (b) presents the experimental results for the opposite power flow when the power is processed from v_{dc-2} to v_{ac}, in mode II. For this case, the measured peak efficiency is equal to 95.5%, at 5 kW, for the output voltage v_{dc-2} varying between 350 V and 380 V. Here is necessary to note that the slight difference between the efficiency of modes I and II is due to the droop control curve which forces the multiport converter to operate with different output voltages at dc grid side (v_{dc-2}).

Fig. 18 (c) presents the results when the ELVDC bus is supplied only by the ac side (v_{ac}). In this case, the power processed is up to 300 W, which is specified for the USB PD output. Due to the reduced power and multiple power processing stages, the efficiency is penalized by losses in the ac-dc stage, resulting in a peak efficiency of 84.9% at 300 W. However, it is also necessary to note that this operation mode only occurs in emergency cases, when there is a blackout on the dc side. For the normal operation of the main dc bus, the power can be processed to ELVDC directly from v_{dc-2}, in operation mode IV. The experimental efficiency is presented in Fig. 18(d), where the peak efficiency equals 96.8%, measured at 300 W.

Fig. 19 presents the power loss distribution for the different cases, according to the operation modes described in Fig. 11. For the operation modes I, and II, the main losses are concentrated in the ac-dc converter, as shown in Fig. 19 (a), and Fig. 19 (b), respectively. For the dc-dc stage, the DAB converter and transformer losses are separated because the transformer plays an important role in the converter losses for all operation modes. In addition, the DAB converter operates with full soft-switching, as described in [10].

For the operation mode III, the dc-dc stages have lower power losses because the DAB is only partially used, as presented in Fig. 19 (c). However, the share of transformer losses is significant because the power converter processes only 300 W.

This is one disadvantage of a multiport converter since the transformer is designed for rated power (5 kW). In some operation modes, the multiport converter could operate with very low power, making core losses dominant.

Fig 19 (d) presents the power distribution losses for operation mode IV. Even though the transformer losses are still significant, avoiding power processing in the ac-dc stage ensures better efficiency in this case.

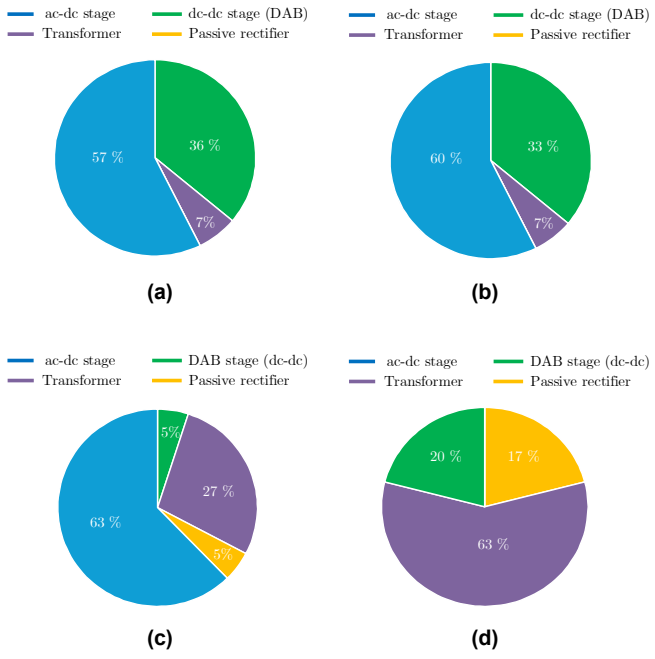


FIGURE 19. Power distribution losses for different operation modes: (a) Mode I – power flow from v_{ac} to v_{dc-2}; (b) Mode II – power flow from v_{dc-2} to v_{ac}; (c) Mode III – power flow from v_{ac} to v_{dc-3}; (d) Mode IV – power flow from v_{dc-2} to v_{dc-3}.

V. CONCLUSIONS

This paper proposes a multiport (ac/dc/dc) converter to address the isolation requirements specified by current standards NPR9090 and Current/OS protocols. According to these standards, galvanic isolation between the ac and dc sides is necessary. Additionally, using an isolated ELVDC bus enhances user safety against electric shocks. Compared to multi-stage, series-connected solutions, the multiport converter offers several advantages, such as a reduced number of components and power processing stages, thus improving overall system feasibility.

The proposed multiport converter features a two-level voltage source converter for the ac-dc stage and a dual active bridge (DAB) with an additional center-tap rectifier to achieve the necessary isolation stages. The magnetically coupled design was addressed. Due to the droop control requirements, the output dc voltage $(v_{dc\text{-}2})$ is variable according to the power processed. To avoid undesirable voltage variations on the ELVDC side, a transformer design is proposed to reduce the coupling between the secondary and tertiary windings as much as possible. Experimental results were presented to compare different transformer designs. Although the ELVDC port is not regulated because this power stage relies on a passive rectifier, decoupling the tertiary and secondary windings, where voltage variations occur, allows for maintaining an appropriate voltage level for the USB PD interface.

Related to the converter efficiency, different operation modes were explained and evaluated. For the main power processing stages, the efficiency of 94.6% and 95.5% was measured for 5 kW of processed power for ac to dc and dc to ac power flow, respectively. For the ELVDC port, the efficiency is reduced when the output port is supplied from the ac grid in case of a dc bus fault. For this case, the experimental efficiency was equal to 84.9%, with the ac-dc converter being the main contributor to the power loss. However, when the ELVDC port is supplied directly from the main dc grid, the power converter efficiency reaches 96.8%, as additional power processing stages are avoided.

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AUTHORS' CONTRIBUTIONS

CARVALHO E. L.: Conceptualization, Formal Analysis, Experimental Validation, Writing – Original Draft, Writing – Review & Editing. **CHUB, A.**: Conceptualization, Formal Analysis, Writing, Review & Editing. **BLINOV, A.**: Experimental Validation, , Review & Editing. **BANAVATH, S. N.**: Conceptualization, Formal Analysis, Investigation, Methodology, Software, Writing – Review & Editing. **VINNIKOV, D.**: Conceptualization, Formal Analysis, Investigation, Methodology, Writing – Review & Editing. Founding Acquisition.

PLAGIARISM POLICY

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BIOGRAPHIES

Edivan Laercio Carvalho received the B.Sc. and M.Sc. degrees in electrical engineering from the Federal University of Technology – Paraná (UTFPR), Brazil, in 2015, and 2018, respectively, and the Ph.D. degree in electrical engineering from Federal University of Santa Maria (UFSM), Brazil. He is currently a Researcher with the Power Electronics Group, Tallinn University of Technology, Estonia. His research interests include high-frequency power converter topologies, net-zero energy buildings, and power management systems.

Andrii Chub received the B.Sc. and M.Sc. degrees in electronic systems from Chernihiv State Technological University, Ukraine, in 2008 and 2009, respectively, and the Ph.D. degree in electrical engineering from the Tallinn University of Technology, Estonia, in 2016. He is currently a Senior Researcher with the Power Electronics Group of Tallinn University of Technology. His research interests include advanced dc–dc converters, energy-efficient buildings, and fault-tolerance of power electronic converters.

Andrei Blinov received the M.Sc. degree in electrical drives and power electronics and the Ph.D. degree, from the Tallinn University of Technology, Tallinn, Estonia, in 2008 and 2012, respectively. He is currently a Senior Researcher with the Power Electronics Group of Tallinn University of Technology. His research interests include the research of switch-mode power converters, new semiconductor technologies, and energy storage systems.

Satish Naik Banavath holds a B.Tech. degree in electrical and electronics engineering from Acharya Nagarjuna University, Guntur, India in 2010, M.E. and Ph.D. degrees in electrical engineering at the Indian Institute of Science, Bengaluru, India, in 2012 and 2018, respectively. From 2012 to 2014, he worked with the Defence Research and Development Organization (DRDO), Ministry of Defence, Government of India, in Bengaluru. Subsequently, he served as a Postdoctoral Fellow at the University of Houston, Houston, TX, USA, from 2017 to 2018. Later, he joined Mahindra Electric Mobility Limited in Bengaluru, where he held the position of Research and Development Manager from 2018 to 2019. Since 2019, he has been an Assistant Professor in the Department of Electrical Engineering at the Indian Institute of Technology (IIT) Dharwad, India.

Dmitri Vinnikov received the Dipl.Eng., M.Sc., and Dr.Sc.techn. degrees in electrical engineering from the Tallinn University of Technology, Tallinn, Estonia, in 1999, 2001, and 2005, respectively. He is currently the Head of the Power Electronics Group of Tallinn University of Technology. He has authored or co-authored four books, five monographs and several book chapters as well as more than 600 published papers on power converter design and development and is the holder of numerous patents and utility models in this field. His research interests include applied design of power electronic systems, renewable energy conversion systems, energy-efficient buildings, reliability and fault-tolerance of power electronic systems.